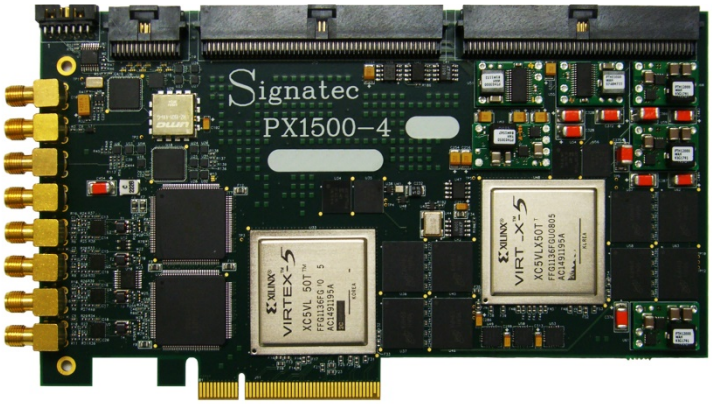
Product Information Sheet

PX1500-4

8-Bit, 4 CH @ 1.5 GS/s or 2 CH @ 3 GS/s, PCIe Digitizer



FEATURES

- 4 Analog Input Channels up to 1.5 GS/s per Channel
- 2 Analog Input Channels up to 3 GS/s per Channel
- 8 Bits of Resolution
- Bandwidth up to 2 GHz
- 2 GB Total Onboard RAM for Sample Acquisition
- 1.4 GB/s Sustained PCIe Data Streaming Rate
- Xilinx Virtex-5 FPGA Processing Option
- FIR Filtering or User Custom FPGA Processing Routines
- Windows Scope App and Complete C SDK Included
- Windows and Linux Operating Systems Supported

APPLICATIONS

- SIGINT
- RADAR
- LIDAR
- Spectroscopy
- Mass Spectrometry – Time of Flight
- RF Communications
- Ultrasound
  - Medical Diagnostics
  - Non Destructive Testing
- Laser Doppler Velocimetry
- High Speed / High Resolution Waveform Capture

OVERVIEW

The PX1500-4 is a four channel waveform capture board that can acquire up to 1.5 GS/s on each channel, or up to 3 GS/s for dual channel operation when ADC data is interleaved. The PX1500-4 analog front end is hardware configured to use either a transformer coupled front end or an amplifier connection. The transformer connection can only be set for an AC-coupled input configuration and has a signal frequency capture range of 5 MHz to 2 GHz. The amplifier connection can be set for either AC or DC-coupled input configuration with a signal frequency capture range up to 1 GHz.

The PX1500-4 is designed to maximize the quality of the captured signal in terms of signal-to-noise ratio and spurious-free dynamic range over a very wide frequency range. For this reason, there are no switch components in the analog signal path or bandwidth limiting programmable gain amplifiers; giving customers the benefit of a nearly direct path to the ADC from either the amplifier or transformer coupled input.

A frequency synthesized clock allows the ADC sampling rate to be set to virtually any value from 200 MHz to 1.5 GHz, offering maximum flexibility for sampling rate selection. This frequency selection flexibility comes at no cost to the acquisition clock quality/performance when locked to either the onboard 10 MHz, ±5 PPM reference clock or to an externally provided 10 MHz reference clock. The ADC may also be clocked from an external clock source.

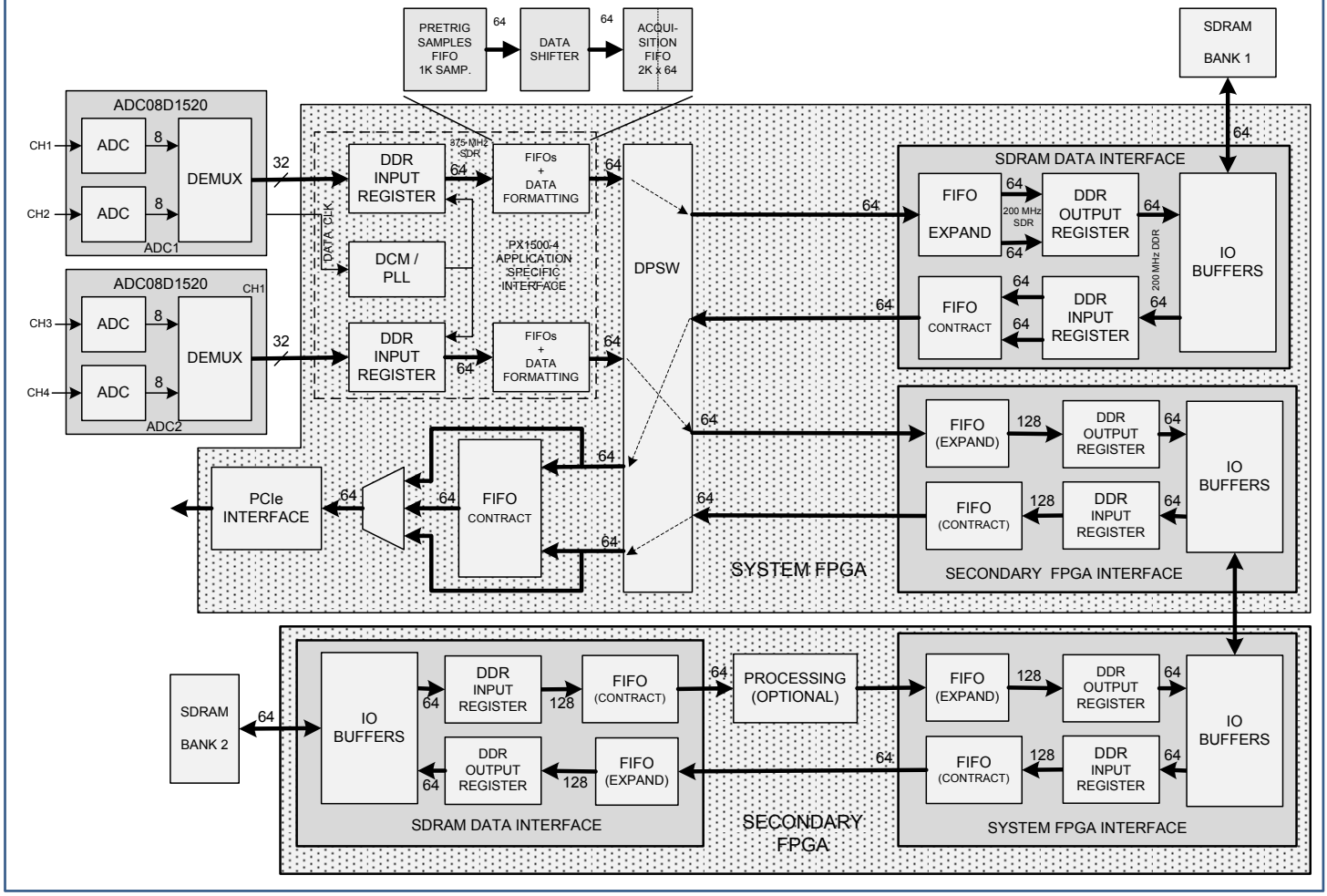
The PX1500-4 has a total of 2 GB memory for onboard sample data storage. Alternatively, PCIe Buffered Acquisition mode utilizes the onboard RAM as a FIFO to provide non-stop continuous acquisition and streaming of sample data to the host PC via the PCIe interface. With PCIe Buffered Acquisition mode, the PX1500-4 can sustain up to a maximum 1.4 GB/s data streaming rate over its PCIe Gen1 x8 interface to the host PC for real-time high-speed processing and/or data recordings.

The PX1500-4 also provides an option for an upgraded secondary Xilinx Virtex-5 SX95T FPGA for embedded signal processing on channels 3 and 4 inputs. FPGA processing models of the PX1500-4 include a FIR Filtering feature standard for these inputs. The processing FPGA is fully end user programmable, allowing for custom developed embedded processing routines.

Up to five PX1500-4 digitizers can be setup for synchronous acquisition operations for a total of 20 input channels by utilizing the separate Signatec SYNC1500 clock/trigger driver source card.

A Windows oscilloscope program, the PX1500 Scope App, allows the operator to view/edit all digitizer hardware settings as well as record and display acquisition data. It is included along with a full complete C SDK for custom application development.

PX1500-4 Functional Block Diagram



Analog Input Front End

The functional block diagram shows a simplified mechanization for the PX1500-4. The analog input circuitry for each of the four channels is identical and each channel input must be set at the factory for either AC or DC coupling with either an amplifier or transformer front end connection. The transformer front end connection can only be used with AC coupling.

The transformer input allows for higher bandwidth frequency operation from 5 MHz to 2 GHz, as well as slightly better performance in terms of SNR and SFDR, with a fixed input voltage range of 700 millivolts peak-to-peak.

The amplifier input provides the ability to capture lower bandwidth frequency operation from DC to 1 GHz, or from 1 MHz to 1 GHz for an AC-coupled configuration, at lower signal levels with a fixed input voltage range of 500 millivolts peak-to-peak.

ADC data can be captured in quad, dual, or single channel modes. The onboard 1 GB SDRAM bank 1 memory is shared for channel 1 and 2 inputs, and the onboard 1 GB SDRAM bank 2 memory is shared for channel 3 and 4 inputs. Data flows through the various circuit functions via a series of self-managed FIFO to FIFO transfers. Optional secondary FPGA processing functions can be inserted into the data flow for channel 3 and 4 inputs.

ADC Clock Circuit

An internal synthesized clock is the primary clock source for the ADCs. This synthesized clock on the PX1500-4 allows for users to dial in any clock frequency from 200 MHz to 1.5 GHz for the onboard ADCs. The ADC clock can also be supplied from the external clock input connector.

If the external clock input is the ADC clock source, it may be divided by any integer value from 1 to 7. For all clock sources the effective digitization rate can be further reduced via sample discarding of the digitized data. This second post-ADC emulated clock division feature can effectively divide down the clock rate by 1, 2, 4, 8, 16 and 32.

With interleaved ADC mode, the active ADCs will run in Dual Edge Sampling (DES) mode in which the ADC's I input will be digitized by both internal converters running in antiphase. This effectively doubles the acquisition sampling rates up to 3 GS/s for single or dual channel modes that are supported on channel 1 and channel 3 inputs only.

The synthesizer clock is locked to a 10 MHz reference clock. The reference clock may be selected from the internal reference or an externally supplied reference clock. The internal reference clock is accurate to better than ±5 PPM. This sets the ADC clock accuracy to also be within ±5 PPM.

External Inputs/Outputs

Besides the input signal channels, the PX1500-4 also provides SMA connections for a clock input, an external trigger input, and a digital input/output signal. The clock input can be used to supply the source clock for the ADCs or a 10 MHz reference clock for the internal synthesized clock. The digital I/O connector supports output modes of 0V, synchronized trigger, ADC clock divided by 8, or 3.3V and an input mode supporting a digital pulse for timestamp request.

Operating Modes

The PX1500-4 has the following operating modes:

- **Standby** – Passive mode with no data activity.
- **RAM Acquisition** –Data is captured into onboard RAM.
- **PCIe Transfer** – Transfer data in onboard RAM to the PCIe bus after a completed RAM Acquisition.
- **PCIe Buffered Acquisition** –Data is simultaneously acquired and streamed to the PCIe bus, using onboard RAM as a FIFO.

Of particular interest is the PCIe Buffered Acquisition mode where the RAM is operated as a large FIFO for acquiring data to the PCIe bus, though the sustained transfer rate to the PCIe interface is limited to 1.4 GB/s. See the following PCIe Interface section for further details.

Triggering

The external trigger input can be used to synchronize the start of data acquisition with an external event. This is a digital input with LVPECL signal level that is terminated to 50 ohms to +1.3V. This is the proper termination for a LVPECL signal source based on +3.3V VCC. The trigger occurs on the positive going edge of the signal.

Acquisition may also be set to occur based on the amplitude level of any of the four input signals exceeding a programmed trigger level. The triggering threshold is a digital value that is compared against the digitized signal. The detection is edge based with either positive or negative excursion being selectable.

Two triggering modes are available: post trigger or segmented. In post trigger mode, following the detection of a trigger signal, all of the active memory is filled. In the segmented mode a separate trigger signal is required to successively fill each memory segment until all of the active memory is filled. PCIe Buffered Acquisition mode can be combined with either of these trigger modes for creating high-speed continuous (gap-free) or triggered/pulsed based data streaming to the host PC.

Up to five PX1500-4 digitizers can be setup for synchronous acquisition operations for a total of 20 input channels by utilizing the separate Signatec SYNC1500 clock/trigger driver source card. The SYNC1500 provides very precise clock and trigger signals distributed to the connected PX1500-4 digitizers simultaneously. Please refer to the Signatec SYNC1500 product data sheet for further details.

Samples Settings

There are several settings that affect the quantity and method of acquiring samples.

Active Memory Size – The number of samples that will be taken after which the memory will be considered “full” and acquisition is terminated. When a full condition is detected, a flag is set which may be read by the PC or software selected to cause a PC interrupt. The amount of memory that is activated for data acquisition may be set from 16 bytes to the full 2 gigabytes in steps of 16 bytes. In PCIe Buffered Acquisition modes it is possible to operate in a “free run” mode whereby streaming data is collected until the digitizer is commanded to terminate the acquisition.

Segment Size – In Segmented Mode, the number of samples that will be taken each time a valid trigger signal is detected.

Pre-trigger Samples – The number of samples that will be recorded into RAM that occurred before the trigger event.

Trigger Delay Samples – The number of samples occurring after the trigger event that will be ignored.

Timestamps

The PX1500-4 can be configured to generate timestamps for certain events. A timestamp is a 64-bit unsigned value that represents a number of clock ticks. Upon transition from Standby operating mode to any acquisition operating mode, the timestamp counter will reset to 0 and increment once per acquisition clock cycle. As timestamps are generated, they are inserted into the Timestamp FIFO. Software can read timestamps from this FIFO as the acquisition progresses or after the acquisition completes. The timestamp mode determines how the PX1500-4 generates timestamps:

Timestamp per segment – Generates a timestamp at the start of each segment acquired while in segmented trigger mode.

Timestamp per external trigger – Generates a timestamp for each pulse received on the external trigger input.

Timestamp per digital IO pulse – Generates a timestamp for each pulse received on the digital I/O connector. This mode is useful if timestamp pulse is independent of the trigger signal, and can be used with GPS cards to correlate absolute time and position to the acquired sample index with the timestamp file.

PCIe Interface

The PX1500-4 implements a PCIe Gen1 x8 lane interface capable of streaming a sustained maximum data transfer rate of 1.4 GB/s with PCIe Buffered Acquisition mode to the host PC for real-time high-speed processing and/or data recordings.

When conducting a sustained continuous or gap free data streaming operation to the host PC, the maximum quad channel sampling rate supported is 350 MHz, the maximum dual channel sampling rate supported is 700 MHz and the maximum single channel sampling rate supported is 1.4 GHz.

When conducting a sustained triggered or pulsed data streaming operation to the host PC, the maximum sampling rates for quad, dual or single channel operation is possible as long as the trigger rate and the number of samples per segment acquired produce an effective total data transfer rate of 1.4 GB/s or less.

FPGA Signal Processing Option

The FPGA processing model version, the PX1500-4-SP95, features an onboard upgraded secondary Xilinx Virtex-5 SX95T FPGA for embedded signal processing on channels 3 and 4 inputs. This processing FPGA then conducts both the data acquisition operation of these channel inputs in addition to the targeted processing routine on the acquired data.

When FPGA processing is enabled, the targeted signal processing routine is conducted and the resulting processed data output is then transferred back to the System FPGA, which can then stream the resulting data to the host PC system via the PCIe interface with PCIe Buffered Acquisition mode.

PX1500-4-SP95 FPGA processing models include the following signal processing routines:

Finite Impulse Response (FIR) Filtering – Provides programmable FIR filtering for channel 3 and channel 4 inputs with the ability to load filter coefficients from a file source for each channel.

The PX1500 Scope App includes an interface to enable FPGA processing and for making settings that apply to the routine.

Custom FPGA Signal Processing Development

The processing FPGA is fully end user programmable, allowing for customized embedded processing routines to be developed and utilized with the PX1500-4-SP95. Signatec provides custom FPGA design services to meet specific application requirements for customers who don't want to program the FPGA themselves. Contact Signatec to discuss specific project requirements, feasibility, and scope for customized solutions.

Alternatively, the optional PX1500 FPGA Development Kit is provided for customers who want to develop their own embedded processing routines.

The Signatec PX1500 FPGA Development Kit requires the end user to have the Xilinx ISE Design Suite software sold directly by Xilinx and provides the native VHDL source code project of the existing PX1500 FPGA processing routines for FIR Filtering. This VHDL source code project serves to demonstrate how to write real-time embedded signal processing routines for the onboard Xilinx FPGA device with its defined interfaces for utilizing the various FIFO, RAM, processing elements, and bus interface resources.

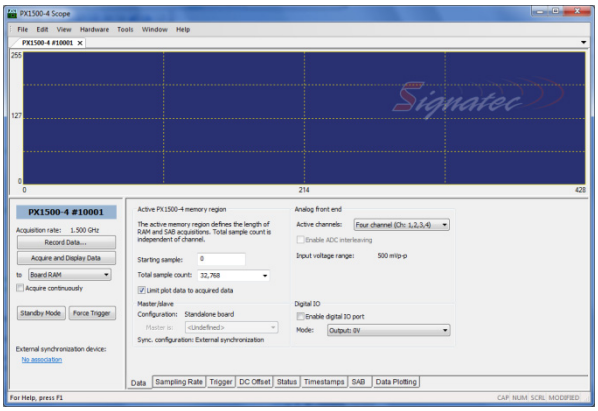
Purchase of the PX1500 FPGA Development Kit includes up to 5 hours of DynamicSignals engineering support. Additional hours of support can be purchased in units of 5-Hour Block Packages.

The custom programmable FPGA logic needs to manage two data interfaces: the acquisition data interface and the user register interface. The acquisition data interface provides data from the PX1500 acquisition circuits to be processed by the user logic in the programmable FPGA. The register interface provides a way for user defined custom parameters to be dynamically set by the host PC system application.

The PX1500 Scope App includes a generic FPGA Processing interface for enabling FPGA processing and to read/write to specific registers for working with the custom user logic in the FPGA. For custom application software development, standard C functions are provided for interfacing with the FPGA registers.

Developed custom user logic firmware is packaged and uploaded to the PX1500-4-SP95 through its PCIe interface to the host PC utilizing the PX1500 Scope App. Alternatively the custom user logic firmware can also be directly loaded through the PX1500-4-SP95 JTAG header utilizing a Xilinx JTAG programmer sold directly by Xilinx.

Scope Application



The PX1500 Scope App software is a virtual oscilloscope application that allows the operator to view or edit all digitizer hardware settings as well as record and display acquisition data.

When the Scope App starts, it will automatically connect to all local PX1500 digitizer devices. Note that when the application starts up, the digitizer hardware is not accessed. This allows the Scope App to run without directly affecting any digitizer operations that may be in progress with other software.

The Scope App may be used to modify any of the various hardware settings that affect how the digitizer behaves. These settings are distributed over the tabbed view at the bottom of the main device form. The main interface is divided into three resizable panels.

The top panel is the 'Scope' panel and is used to display digitizer acquisition data, data recording snapshots, and previously recorded data files. The plot area can display multiple channels of independent or interleaved data of varying sample sizes (8-, 12-, 14-, 16-, 32- bit) and types (signed, unsigned, floating point) simultaneously. The default units displayed for the data are time (horizontally) and voltage (vertically), with optional settings for sample number (horizontally) and ADC value (vertically). Plotted data is read-only; there are no facilities to modify data with this interface.

The 'Data Plotting' tab in the Settings area controls many of the data plotting parameters. This includes scaling parameters, channel visibility, and channel source information. In addition, the mouse may be used to alter the horizontal and vertical scaling of the data as well as panning through the data.

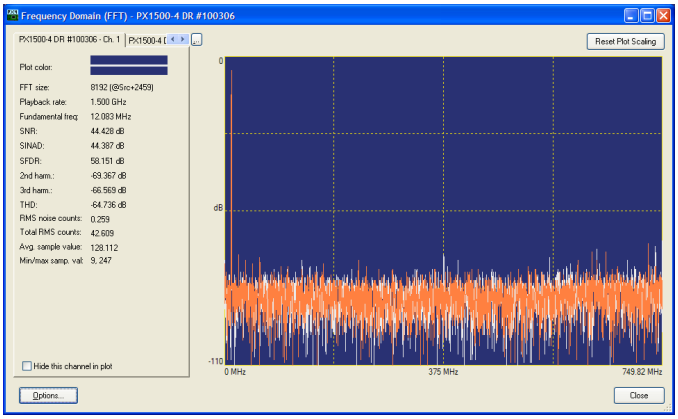
The bottom-left panel is the 'Control' panel and is used to start and stop data acquisitions and recordings. The options on this panel have to do with controlling the digitizer operating mode such as acquire data for a single instance, acquire data continuously, initiate a recording data session, issue software trigger, or enter standby mode.

The bottom-right panel is the 'Settings' panel and is a tabbed view with various tabs that control the various digitizer hardware settings. Certain tabs are only displayed if the underlying digitizer device supports those features. The Scope App allows for saving all digitizer hardware settings to a file that can be opened and applied to the hardware at a later time, thus saving time from manually re-applying settings for repetitive configurations. The tabbed interface settings include:

Data	Settings that control how much data to acquire for RAM acquisitions as well as analog front end settings and digital I/O settings.
Sampling Rate	Settings that affect the digitizer acquisition clock, which defines the sampling rate.
Trigger	Settings that affect the digitizer trigger. These settings relate how data is collected relative to external events.
Status	Contains an interface to read hardware status items with version and configuration information for various hardware, firmware, and software entities displayed.
Timestamps	Settings that affect timestamp modes and operations.
Data Plotting	Settings that affect how data is displayed in the Scope panel. Also provides interface for opening previously saved signal data files into the scope.

Scope App – FFT Analysis

The Scope App has the ability to do FFT analysis on digitizer (or file) data. FFT operations are performed on data sources that are currently displayed in the Scope panel and are displayed on the Frequency Domain (FFT) window.



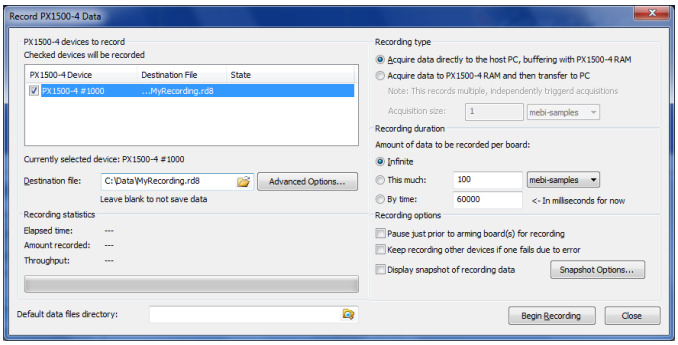
The FFT window is divided up into two regions. The left side is a tab control that contains various FFT and time-domain statistics. There is one tab for each channel of data. The right side contains the frequency domain plots of all channels.

Reported FFT and time-domain statistics include FFT Size, Playback Rate, Fundamental Frequency, SNR, SINAD, SFDR, 2nd Harmonic, 3rd Harmonic, THD, RMS Noise Counts, Total RMS Counts, Average Sample Value, Min/Max Sample Value, and Peak Frequencies.

FFT option settings include changing the FFT size, Windowing method used with options of Rectangular, Hanning, Hamming, and Blackman-Harris, controlling where the source time domain data will be obtained from (beginning of data source, selection on time-domain plot, or from specific given offset into the data source), enabling FFT averaging to average out any ambient noise in the frequency domain with averaged tracked resultant magnitude-squared FFT results shown, enable tracking of peak FFT frequencies, and ignore a specified percentage of noise margin outside of the fundamental frequency.

Scope App –Data Recordings

The Scope App Record Data interface is used to conduct data acquisition recordings.



The Scope App supports two types of data recordings:

Acquire Data Directly to the Host PC, Buffering with device RAM – Used to record one long continuous stream of gap-free data, or one long continuous stream of discrete data segments if in segmented mode (triggered/pulsed based capture), utilizing PCIe Buffered Acquisition mode. This is the most common type of data recording. In this mode the underlying host PC system and targeted data storage location must be able to sustain the acquisition streaming data rate, or a FIFO overflow error condition will occur and the recording stopped. Signatec also provides complete PC signal recording systems that are specifically tailored for real-time data streaming recording applications that require a guaranteed continuous transfer rate with no missing data; please refer to the Signatec Sig-Station and Signal Recording Systems product catalogs for further details

Acquire Data to RAM and then Transfer to PC – Used to record a series of non-contiguous acquisitions with PCIe Transfer mode. First, new data is acquired to RAM and then after the acquisition has completed, the data is transferred to the host system. Note that while data is being transferred to the system, no new data is being acquired. This type of recording is useful in cases where the targeted full acquisition rate may be too fast to support PCIe Buffered Acquisition mode.

The duration of the data recording to be conducted can be set to:

Infinite – Recording goes on indefinitely until manually stopped by the operator or targeted data storage location reaches full capacity.

Data Amount – Records the amount of data specified in total number of gibi-samples, mebi-samples, kibi-samples, or samples. Note: gibi-, mebi-, and kibi- prefixes denote 1073741824 (2^{30}), 1048576 (2^{20}), and 1024 (2^{10}) respectively.

Time – Converts the given total time specified in number of milliseconds into an equivalent sample count (which is a function of acquisition rate) and then records that much data. Note that the time amount specified is the entire time of recorded data, not including the time to wait for a trigger event.

Regardless of the recording duration type selected, a recording may be manually stopped anytime by clicking the 'Stop Recording' button in the Recording window.

Snapshots of the recording data can be displayed in the scope plot area during live recordings. An 8192 point snapshot is obtained roughly once a second by default. The snapshot setting can be modified to specify the desired targeted size in samples and desired targeted frequency in milliseconds.

Recording statistics are displayed during the live recording detailing the current elapsed time, the current amount recorded, and the current total data throughput rate.

There are various destination file data saving options that include: Append Data if it Already Exists, De-Interleave Data into Separate Files, Span Data Over Multiple Statically Size Files, Convert Data to Signed Format before Writing, Leave Room for Application Specific Data, Save Data as Text, and Add Operator Notes to Signatec Recorded Data Context (SRDC) Information.

The native file format for recorded PX1500 acquisition data is the RD8 file format. The RD8 moniker is derived from "Raw Data 8-bit" and is identified by the '.rd8' file extension. RD8 files are raw binary files that contain only acquisition data; there is no file header or additional information in the file. The first byte of the file is the first data sample. Samples in .rd8 files are 8-bits in size. By default, multi-channel data is saved in interleaved format (i.e. Ch1, Ch2, Ch3, Ch4, Ch1, Ch2, Ch3, Ch4, Ch1, Ch2, Ch3, Ch4, etc.). Samples are stored in little-endian format; this is the native binary format for the x86 platform.

The simple raw data file format has two big advantages. First, it's very fast to write these files since data is written to the file exactly as it is received from the Signatec digitizer. If the underlying file system (PC host platform and storage destination) can keep up with the data rate, data can be streamed from the digitizer card to the file at the highest streaming recording rate supported. The second advantage is that this file format is very generic which makes it easy for other software to import and utilize the data, such as LabVIEW or MATLAB.

Signatec data samples are unsigned values and the recording RD8 data file can be read as binary data into MATLAB using the "uint8" to import the data as unsigned 8-bit format. Once the data is read into MATLAB, subtract 128 from each sample value to center the data around 0; as unsigned samples have:

- Maximum possible data sample value: 0xFF == 255
- Midscale sample value: 0x80 == 128
- Minimum possible data sample value: 0x00 == 0

The RD8 file format does not store any context information about the details of the data in the file. Therefore by default the Scope App also generates a Signatec Recorded Data Context (SRDC) file. A SRDC file is a small generated XML-based formatted file that contains information about the associated RD8 data file that includes items such as channel count, input voltage range, sampling rate, source digitizer, operator notes, or any other user-defined data. SRDC files are identified by the '.srdc' file extension and reside in the same storage location of the RD8 file when generated. SRDC files are easily read by any XML-aware software.

The Scope App can be used to open and view previously saved data recording files in the Scope Panel on the "Data Plotting" tab and to view the SRDC contents about the recorded data file.

SOFTWARE DESCRIPTION (Continued) and ATTENUATORS

Software Development Kit for C/C++

Complete documented Application Programming Interfaces (APIs) with C/C++ callable function libraries for the PX1500-4 are included for custom software development.

In addition, complete fully commented source code for the Scope App is included along with individual project examples that illustrate how to use the function libraries for building custom applications.

Linux Software

The PX1500-4 is also supplied with Linux software that includes:

- Product kernel mode hardware drivers supporting both 32-bit and 64-bit Linux operating systems.
- User Mode Library – Full software C/C++ function library API for custom application development.
- Documented example application C source code projects that demonstrates: RAM acquisition and data transfer, acquisition recording with single device, and recording data using Session API.

PX1500 Linux software is validated with Red Hat Enterprise Linux and Ubuntu Linux distributions. In general, user mode code can typically be ported to other Linux distributions as well.

Optional Software Packages

Optional software packages available for the PX1500 include:

LabVIEW Interface	LabVIEW Interface software includes supplied LabVIEW virtual instruments (VIs) for the PX1500 with full VI reference documentation for use within the LabVIEW environment.

Software Updates

Future software and manual updates are available for download for registered users for the lifetime of the PX1500 product at no additional charge.

Attenuators

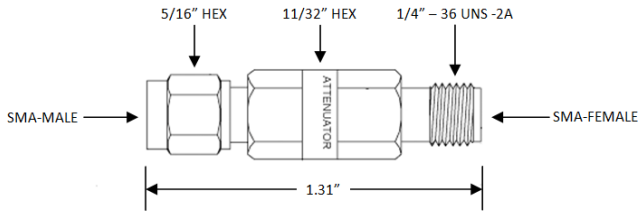
Use the following part number format to order optional SMA attenuators for use with the PX1500-4:

SMA Attenuator Part Number Format: **662-*dB*-1**

Insert the target attenuation value (see table below) in place of ***dB***.

EXAMPLE: **662-6-1** for 6 dB

The attenuator specifications are as follows:



Electrical Specifications					
Avg. Power (Watts)	Peak Power (Watts)	Freq. (GHz)	VSWR (Max)	Attenuation Value (dB)	Attenuation Tolerance
2	500	Hz-2.0 2.0-4.0	1.15:1 1.25:1	3, 6, 10, 20	± 0.6 dB ± 0.8 dB
		Hz-2.0 2.0-4.0	1.25:1 1.35:1	30	± 1.0 dB ± 1.5 dB

Mechanical Specifications	
Connectors	Brass Albaloy Plated
Male Pin	Brass Gold Plate
Female Pin	Beryllium Copper Gold Plate
Housing	Brass Albaloy Plate
Insulator	PTFE Virgin Electrical Grade
Operating Temperature	-67° F to +185° F / -55° C to +85° C
Weight	62 oz / 1.76 kg

PX1500-4 SPECIFICATIONS

External Signal Connections

Analog Inputs – 4	: SMA
Clock Input	: SMA
Trigger Input	: SMA
Digital Input/Output	: SMA

Analog Inputs – Amplifier Front End

Full-Scale Volt. Range	: 500mV peak-peak
Impedance	: 50 ohms
Bandwidth	: 1 MHz to 1 GHz (AC-Coupled), DC to 1 GHz (DC-Coupled)
SNR (DC – 500 MHz)	: 42 dB
SFDR (1 – 500 MHz)	: 53 dB

Analog Inputs – Transformer Front End

Full-Scale Volt. Range	: 700mV peak-peak
Impedance	: 50 ohms
Bandwidth	: 5 MHz to 2 GHz (AC-Coupled)
SNR	
(DC – 500 MHz)	: 44 dB
(@ 1 GHz)	: 42 dB
(@ 1.5 GHz)	: 40 dB
SFDR	
(5 MHz – 1 GHz)	: 55 dB
(@ 1.5 GHz)	: 48 dB

External Trigger

Signal Type	: LVPECL (3.3V Logic)
Impedance	: 50 ohms to +1.3V

Internal Synthesized Clock

Frequency Range	: 200 MHz to 1.5 GHz
Resolution	: better than ±62.5 PPM
Accuracy	: better than ±5 PPM

External Clock

Signal Type	: sine wave or square wave
Coupling	: AC
Impedance	: 50 ohms
Termination	: Ground or +1.3V
Frequency	: 200 MHz to 1.5 GHz
Amplitude	: 800mV (-300/+1200)
Clock Dividers	: 1 to 7

Post ADC Clock Divider

Divider Settings	: 1, 2, 4, 8, 16, 32

Reference Clock

Internal	: 10 MHz, ±5 PPM max.
External	: 10 MHz, ±50 PPM max. (required for lock)

Digital Input/Output

Type	: TTL logic level
Max. Frequency	: 200 MHz
Connection	: 100 ohms to FPGA I/O
Output Modes	: 0V, Synchronized Trigger, ADC Clock ÷ 2, 3.3V
Input Modes	: Digital pulse for timestamp request

Trigger Modes

Post Trigger	: single start trigger fills active memory
Segmented	: start trigger for each memory segment

Trigger Options

Pre-trigger Samples	: samples prior to trigger are stored; 16k max.; total all channels
Trigger Delay Samples	: delay from trigger to data storage; Up to 64k digitizer clock cycles max.

Memory

Total Size	: 2 GB
Segment Size	: Up to 512 Megasamples
Segment Re-Arm Time[1]	: 150 nanoseconds
Addressing	: DMA transfer from starting address

Power Requirements

+3.3V	: 3.3 Amps max.
+12V	: 1.0 Amps max.

Absolute Maximum Ratings

Analog Inputs	: ±3.5V
Trigger Input	: -0.2V to +4V DC
Clock Input	: 5V peak-peak
Operating Temperature	: +32°F to +122°F / 0°C to 50°C
Storage Temperature	: -4°F to +158°F / -20°C to +70°C
Operating Relative Humidity	: 10% to 90%, non-condensing
Operating Vibration	: 0.25 G, 5 Hz to 500 Hz
Operating Shock	: 2.5 G, 11 ms, ½ sine
Board Dimensions	: 7.5" L x 4.3" H x 0.75" W 190.5 mm L x 109.22 mm H x 19.05 mm W
Regulatory Information	: RoHS Compliant

Notes:

1. In segmented mode, time from the end of a segment until a trigger will be accepted to begin another segment acquisition.

PX1500-4 ORDERING INFORMATION

Part Number Configuration

The PX1500-4 part number nomenclature for ordering is as follows:

PX1500-4-[*FPGA*]-[*Coupling 1234*]-[*Front End 1234*]-[*Multi-Card SYNC*]

[*FPGA*], required to select one of the following options:

DR = No Onboard Programmable FPGA

SP95 = Onboard Secondary Virtex-5 SX95T Programmable FPGA (94,208 Logic Cells / 8,784 kbits Block RAM / 640 DSP Slices) Includes FIR Filtering FPGA Routine for CH3 and CH4

[*Coupling 1234*], required to specify for each channel input:

Each Channel can be independently configured for either "AC" or "DC" Coupling. Specify the desired Coupling setting for each channel by using the following alpha characters in the sequence of channel numbers 1-4 without any spaces or dashes between each channel designator:

A = AC Coupled Channel
D = DC Coupled Channel

[*Front End 1234*], required to specify for each channel input:

Each Channel can be independently configured for either "Amplifier" or "Transformer" front end connection. Specify the desired front end connection setting for each channel by using the following alpha characters in the sequence of channel numbers 1-4 without any spaces or dashes between each channel designator:

A = Amplifier Front End Connection Channel with Bandwidth of 1 MHz to 1 GHz (AC-Coupled) or DC to 1 GHz (DC-Coupled)

X = Transformer Front End Connection Channel with Bandwidth of 5 MHz to 2 GHz (AC-Coupled). Transformer option is NOT available for DC-Coupled channels.

[*Multi-Card SYNC*], not required – ONLY specify if needed:

SY = Planned PX1500-4 Multi-Card Operations with SYNC1500. Requires purchase of separate SYNC1500 card to provide precise simultaneous clock and trigger signal distribution to each connected PX1500-4 digitizer. The SYNC1500 supports up to five connected PX1500-4 digitizers for a total of 20 input channels for synchronous acquisition operations. This option is NOT required for standalone independent operation of multiple PX1500-4 cards.

Part Number Order Examples

The following are some valid part number ordering examples (this listing does not depict all possible configurations):

PX1500-4-DR-AAAA-AAAA = PX1500-4 with No Programmable FPGA, AC-Coupling for all 4 input channels, Amplifier front end for all 4 input channels

PX1500-4-DR-AADD-XXAA = PX1500-4 with No Programmable FPGA, AC-Coupling for Channels 1 & 2, DC-Coupling for Channels 3 & 4, Transformer front end for Channels 1 & 2, Amplifier front end for Channels 3 & 4

PX1500-4-SP95-DDDD-AAAA = PX1500-4 with Programmable SX95T FPGA, DC-Coupling for all 4 input channels, Amplifier front end for all 4 input channels

PX1500-4-SP95-ADAD-XAXA = PX1500-4 with Programmable SX95T FPGA, AC-Coupling for Channels 1 & 3, DC-Coupling for Channels 2 & 4, Transformer front end for Channels 1 & 3, Amplifier front end for Channels 2 & 4

PX1500-4-SP95-DADA-AXAX-SY = PX1500-4 with Programmable SX95T FPGA, DC-Coupling for Channels 1 & 3, AC-Coupling for Channels 2 & 4, Amplifier front end for Channels 1 & 3, Transformer front end for Channels 2 & 4, Multi-Card Synchronous Operation with separate SYNC1500

Documentation & Accessories

The PX1500-4 is supplied with a comprehensive operator's manual distributed with the software, which thoroughly describes the operation of both the hardware and the software. Also supplied are four four-foot coaxial cables with SMA to BNC connectors. Additional cables may be purchased separately. Supplied software contains:

- Windows 32-bit/64-bit Drivers and Scope App Software
- Complete Software Development Kit for C/C++ with Source Code Examples
- Linux 32-bit/64-bit Drivers and Example Projects

Product Warranty

All Signatec products carry a standard full 2-year warranty. During the warranty period, DynamicSignals will repair or replace any defective product at no cost to the customer. Warranties do not cover customer misuse or abuse of the products.

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