Model 3939-Z2A

Byte-serial, Fiber Optic U-Port Adapter

INSTRUCTION MANUAL

August, 1989

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JRH:rem

Byte-serial Fiber-optic U-Port Adapter

Adds fiber-optic isolation to the Serial Highway

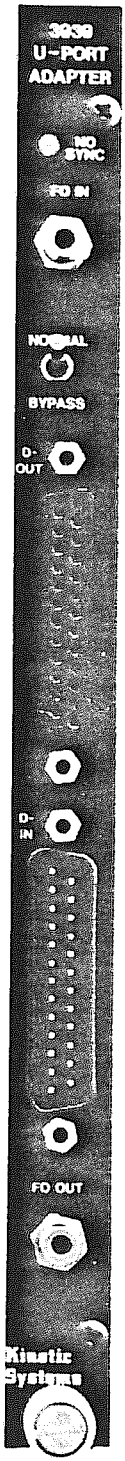
3939

Features

- **Fiber optic cable isolation of CAMAC Serial Highway**
- **Operates in byte-serial mode with a single fiber optic cable loop**
- **Options available for maximum cable lengths of one kilometer and three kilometer**
- **Includes strap-selection for 5, 2.5, and 1 megabyte per second**
- **Unique clock restorer circuit allows five megabyte operation with up to 62 remote crates**
- **External batteries can be used for power-down backup**

Typical Applications

- **Isolated fiber optic highway for Serial Highway Drivers and Type L-2 serial crate controllers**
- **Systems requiring excellent immunity from electromagnetic or electrostatic interference**
- **Remote systems operating at a high potential difference**
- **Systems requiring maximum Serial Highway data throughput**



General Description *(Product specifications and descriptions subject to change without notice.)*

The 3939 is a single-width U-Port adapter module used in CAMAC Serial Highway systems operating in byte-serial mode to five megabytes per second. A unique clock restorer allows full five megabyte per second operation with up to 62 remote crates. U-Port adapter options allow choice of a maximum fiber optic cable length of one kilometer or three kilometers.

When the CAMAC Serial Highway system is operated in byte-serial for maximum data rate, the output D-port from the serial driver (SD) or serial crate controller (SCC) provides one balanced pair for clock and eight pairs for the associated data byte. The 3939 transmitter serializes each byte and transmits the data at ten times the SD clock rate over a single fiber optic cable. The downstream 3939 receiver converts this serial word to a clock and eight data bits for presentation to the SCC or SD input D-port.

The 3939 can be used with the 3952 Type L-2 serial crate controller or with the 3992 serial driver.

Option Summary

Model	Wavelength	Fiber Optic Cable		Maximum Distance
		Model	Core Diameter	
3939-Z1A	820 nanometers	5802-Cxyz	100 micrometers	1 kilometer
3939-Z2A	820 nanometers	(Note 4)	(Note 4)	1 kilometer
3939-Z1C	1300 nanometers	5802-Exyz	50 micrometers	3 kilometers

Notes:
1. Because of the different wavelength used, the Z1C version of the 3939 is not compatible with the Z1A or Z2A versions. Contact the factory for methods of combining them on the same highway.
2. The 5802-Cxyz cable can be used with the 3939-Z1C provided that the length is one kilometer or less.
3. A full 5-megabyte per second operating rate can be used to the maximum distance shown.
4. The 3939-Z2A can be used with 50, 62.5, 85, and 100 micrometer core cable. Refer to the 1730-Series UPA and 5800-Series Cable Assemblies data sheets for additional information and limitations.

A 3939 U-Port system can generally operate at full speed with D-Port SCC clusters using 3952s, provided that all crates in a cluster are in the same rack or equipment bay.

3939 *(continued)*

With power applied to the 3939, it can function as a highway repeater, controlled by the front-panel BYPASS switch or the bypass bit from an L-2 SCC. The BYPASS switch can isolate the D-Port cabling and SCCs from the highway. If power is lost to an L-2 SCC, the SCC asserts its bypass bit to the 3939. If battery backup is provided, highway integrity is maintained.

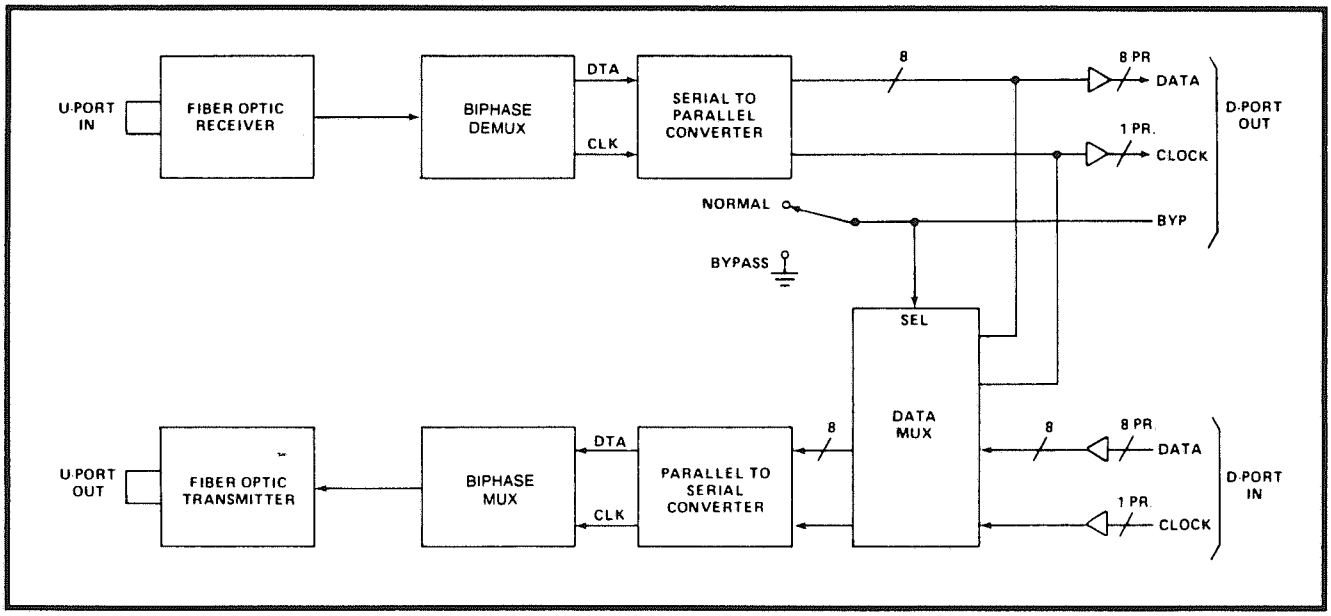
The 3939 contains a 36-contact rear PC connector for connections from an external power source. Plus and minus six volts are required with a tolerance of ±5%. The external supply must be capable of providing the operating current noted below. The 3939 provides an open-collector POWER STATUS signal on the rear I/O connector.

The 3939 normally operates at five megabytes per second. Strap-selection is provided for 2.5 and 1 megabyte per second operation. These speeds may be required in mixed systems where the "twisted-pair" portion of the highway limits the maximum speed.

A NO-SYNC LED on the front-panel aids in identifying highway problems. This LED signal, extended by a one-shot, indicates that a no-sync condition exists (even if momentary) in the fiber optic Serial Highway stream. When in the no-sync state, the 3939 disables its fiber optic transmitter to prevent false crate controller operation in a downstream crate.

Two D-Port cable assemblies included with each 3939 connect to a 3992 Serial Highway Driver or 3952 Serial Crate Controller. Each cable assembly contains a DB25P connector at one end and a DB25S connector at the other end and is 0.25 meters long (Model 5852-F25K). For applications where more than one SCC is used with a single 3939 (crate cluster), please contact the factory for information regarding the appropriate cables for such use.

Simplified Block Diagram



Power Requirements

+6 volts:	1100 mA
–6 volts:	800 mA

Ordering Information

Model 3939-Z1C U-Port Adapter, byte-serial, fiber optic, 1300 nm operation

Model 3939-Z2A U-Port Adapter, byte-serial, fiber optic, 820 nm operation

Related Products

Fiber Optic Highway Cables	Please refer to OPTION SUMMARY on this data sheet.
Model 5960-Z1B	36-contact edge connector (needed if battery backup is provided)

Model 3939-Z2A

PERFORMANCE SPECIFICATIONS

Parameter	Conditions	Min	Typ	Max	Units
Optical Output	50 um/.21 NA Fiber	-21		-14	dBm
Optical Output	62.5 um/.29 NA Fiber	-16		-09	dBm
Optical Output	100 um/.3 NA Fiber	-11		-04	dBm
Output Wavelength			820		
Optical Input	50-100 um Core Dia. .2 - .3 NA Fiber BER = 10^{-9}	-29		-08	dBm
Dynamic Range		21			dBm
Input Wavelength			820		nm

STRAP OPTIONS

Refer to Figure 3 for the board location of the following straps:

1. Transmitter Data Rate: Selects 1, 2.5 or 5 MHz byte D-Port IN rate.

2. Receiver Data Rate: Selects 1, 2.5 or 5 MHz byte D-Port OUT rate (normally set the same as Transmitter Data Rate).

3. Transmitter Symmetry: Compensates for transmitter circuit delay variations. This strap is set at the factory and should not need to be moved.

4. SCC/DRIVER: This strap controls the type of data stream bypass that will occur if a bypass signal is present. When using the 3939 with a Serial Crate Controller, the strap should be in the SCC location. If the 3939 is being used as the front end of a Highway Driver, it should be in the "D" location.

BYPASS

The Model 3939 Fiber-Optic U-Port can be placed into the Bypass mode by a front panel switch, by the Serial Crate Controller (SCC), or by the Serial Driver. With the SCC/DRIVER strap option in "SCC" the Crate Controller, through pin 24 of J1, can bypass fiber-optic incoming data through the receiver, out register "AG", to the transmitter shift register "AC", and out the fiber-optic transmitter. With the SCC/DRIVER strap in "Driver", byte data at J2 D-IN is passed to J1 D-OUT (Used to check D-cables at the driver.). When bypassed by the front panel switch, the above mentioned SCC/DRIVER strap option data routing is true and the byte clock on the D-Port OUT is inhibited. If the 3939 is bypassed by the SCC, the byte clock and byte data are monitored by the SCC for a possible unbypass command. When the 3939 is used with an SCC cluster (Figure 1), the 3939 will unbypass only when all the crate controllers in the cluster have received an unbypass command.

POWER FAIL

A POWER STATUS signal and voltages for battery charging are provided on the rear I/O connector.

With 5 volts and -5 volts present on the 3939, transistors Q1 and Q2 are biased to turn Q1 on, pulling I/O edge connector pin 1R to ground. Loss of either 5 volts or -5 volts, causes Q1 to turn off and connector Pin 1R to float. Plus 24 volts and -24 volts are routed to the I/O connector and used for battery charging. Both 24 volt outputs are fused at 1 amp.

NO-SYNC LED

The NO-SYNC LED signal, extended by a one-shot timer, indicates the 3939 is unable to frame the incoming fiber-optic serial data into byte serial D-Port data. When a no-sync condition exists, the byte clock to the SCC is inhibited and the transmitting LED is held-off. This prevents the SCC from possibly syncing to unframed data.

OPERATING SPEED

The 3939 will operate at three (3) strap-selectable speeds. When selecting either 5 MHz, 2.5 MHz or 1 MHz byte operation, both the transmitter and receiver strap must be moved (Figure 3). No other adjustments are required.

When used at speeds above 1 MB, the clock source must be 2.5 MB or 5 MB, plus or minus one percent for reliable operation. All KineticSystems' drivers (strapped for "crystal") meet this requirement.

CONNECTIONS

The 3939 is connected to an SCC (such as the KineticSystems Model 3952) or a driver (3992, 3994, etc.) by connecting the 3939 D-OUT connector to the D-IN connector of the SCC or SD, and by connecting the SCC or SD D-OUT connector to the D-IN connector of the 3939, using a byte-serial cable such as Model 5852-Fxyz. Fiber-optic cable 5802-Exyz or 5802-Cxyz is used to chain the FO-OUT connector of the 3939 to the FO-IN connector of the next 3939 in the system. Appropriate connectors must be used to achieve the coupled power and receiver sensitivity specifications. When using Type II FSMA connectors, a plastic half sleeve must be used to center the ferrule in the device mount.

If a cluster of D-Port connected SCCs is used (Figure 1), then the 3939 D-OUT is connected to the D-IN of the first Crate Controller, and the D-OUT of the last SCC in the cluster is connected to D-IN of the 3939.

The 3939 may be used with a mixture of KineticSystems Model 2958 byte-serial U-Port Adapters when connected as shown in Figure 2.

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3939 TUNING PROCEDURE

Equipment Required

- Tektronix 100 MHz scope Model 465B or equivalent.
- Two Tektronix P6131 scope probes or equivalent.
- Simpson Model 463 digital voltmeter or equivalent.
- KineticSystems Model 3992 Serial Driver.
- Three (3) meter length 5802E fiber-optic cable.
- Short 25-Pin byte-serial cable.

Setup

1. Strap the Model 3992 serial driver for 2.5 MHz byte operation.
2. Place the Model 3939 on an extender.
3. Cable D-OUT of the 3992 to D-IN of the 3939.
4. Cable FO-OUT of the 3939 to FO IN of the 3939.

Clock Restorer Adjustment

1. Connect scope Channel A to TP3.
2. Connect scope Channel B to I.C. "U" pin 9.
3. Ground scope probes to GND points.
4. Synchronize the scope to Channel A.
5. Strap the 3939 for 2.5 MHz operation.
6. Adjust L3 to align the clock signal of Channel A with the clock signal of Channel B.
7. Strap the 3992 and 3939 for 5 MHz byte operation.
8. Adjust L4 to align the clock signal of Channel A with the clock signal on Channel B.

VCO Adjustment

1. Strap the 3939 for 5 MHz operation.
2. Measure the voltage difference from TP7 to GND.
3. Adjust C30 for 1.90 volts ±.05V.

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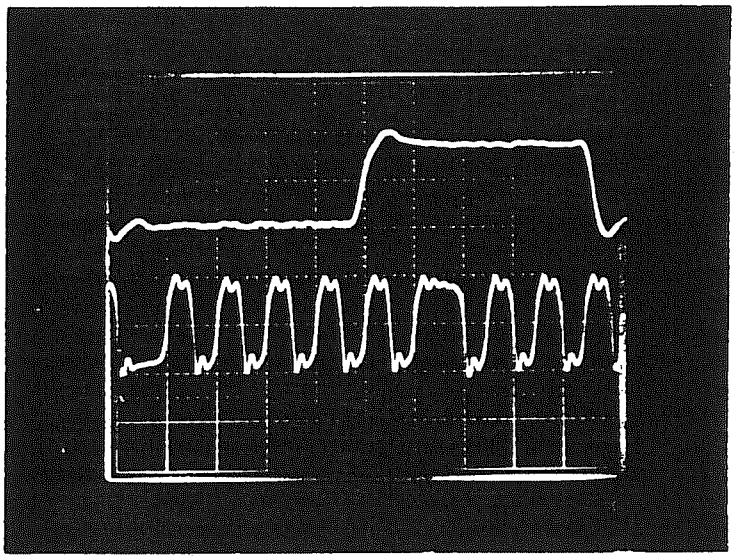
Transmitter Symmetry

1. With scope Channel B, look at TP5 (transmitter output). See Photo 1.

2. Strap TSYM for equal positive and negative pulses.



BYTE CLOCK TP3

WAIT BYTE TP5

20NS/CM
PHOTO 1: WAIT BYTE AT TP5

Receiver Adjustment

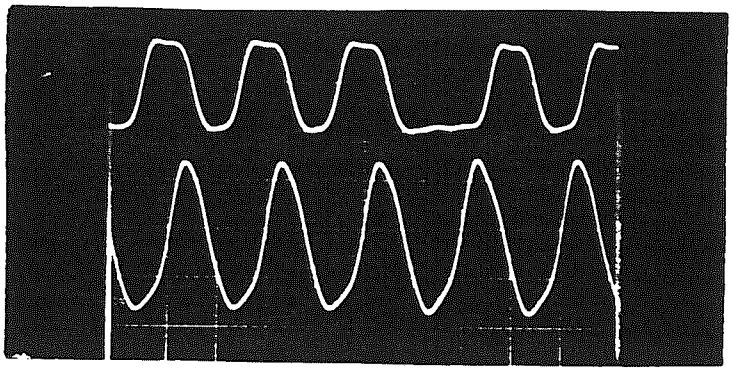
1. Connect FO-OUT to FO IN using three (3) meters of 5802E fiber-optic cable.

2. Synchronize the scope EXT input to TP3 (Byte Clock).

3. Attach scope Channel A to TP1 (Biphase Data).

4. Attach scope Channel B to TP2 (Clock).

5. With the 3939 strapped for 5M byte operation and the scope time-base set at .1 US x 10, adjust C31 to center the positive transition of the clock within the second half of the data cell time (see Photo 2).

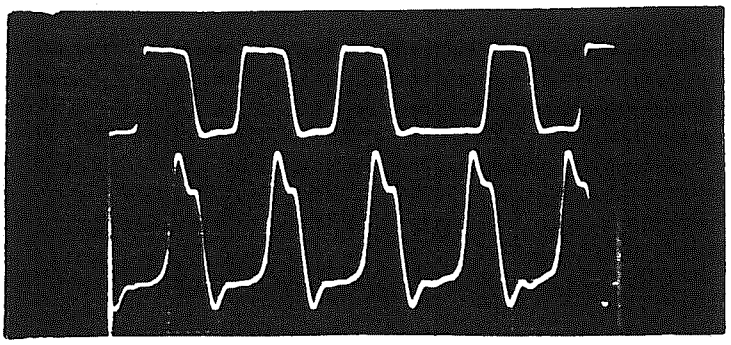


BIPHASE DATA TP1

CLOCK TP2

10NS/CM
PHOTO 2: 5M BYTE OPERATION

6. Strap the 3939 and 3992 for 2.5M byte and check that the positive clock transition is approximately centered within the second half of the data cell (see Photo 3). C31 may be adjusted slightly but 5M byte operation must then be rechecked.



BIPHASE DATA TP1

CLOCK TP2

20NS/CM
PHOTO 3: 2.5M BYTE OPERATION

7. Strap the 3939 and 3992 for 1M byte and again check for proper clock alignment. DO NOT ADJUST C31.

The 3939 is now adjusted for proper operation at all three (3) of its operating frequencies.

TRANSMITTER SECTION

The transmitter section of the 3939 Fiber-Optic U-Port converts the 8-bit byte data from the D-Port IN, to 10-bit serial byphase data, and outputs this data through the FO OUT connector at ten times the byte clock frequency.

The transmitter section consists of four main parts.

1. The clock/counter
2. The parallel to serial converter
3. The NRZ to Manchester (Biphase) encoder
4. The Fiber-Optic transmitter

Clock/Counter

The fiber-optic transmitter clock is required to be ten times the frequency of the D-Port IN byte clock and must be locked to the D-Port clock. A Basic phase-locked loop (Figure 4) is used in the 3939 to fulfill this requirement. When operating properly, it will acquire lock-on to the incoming byte clock, track it in frequency, and exhibit a fixed-phase relationship relative to the byte clock.

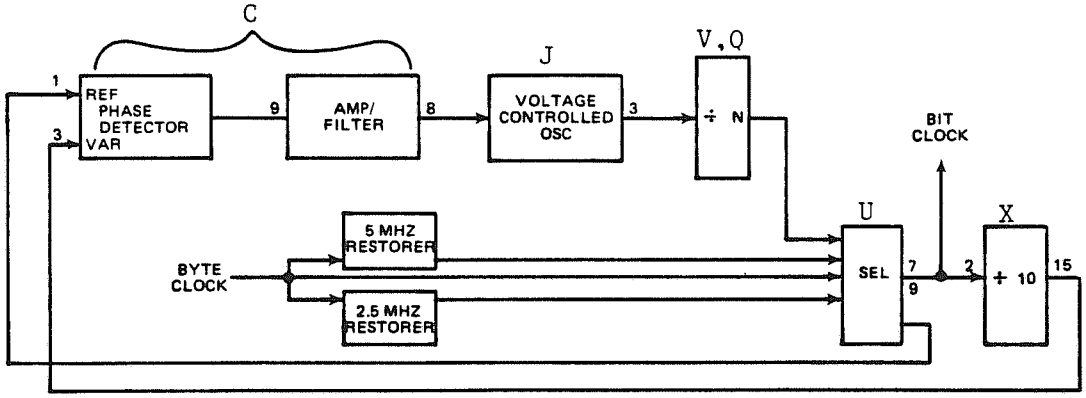


Figure 4

The loop consists of a phase detector, amplifier/filter (chip "C"), voltage-controlled oscillator (chip "J"), and counters (chips "V", "Q", "X") which reduces the VCO 50 MHz to the byte clock frequency. This circuitry appears and acts like a unit gain feedback loop. The controlled variable is phase; any error between byte clock frequency and bit clock frequency ÷N is amplified and applied to the VCO in a corrective direction.

The clock signal (refer to drawing D 5535) from the byte-clock differential receiver is fed into a 5 MHz and a 2.5 MHz clock restorer and also directly into chip "U".

The 5 MHz restorer consists of a parallel resonant tank C4 and L4 and differential amplifier "F" output pin 4. Tuned tank C3 and L3 along with differential receiver "F" output pin 9 make up the 2.5 MHz restorer.

Clock selector "U" selects one of three (3) operating frequencies. Chip "U" pin 9 outputs the selected incoming byte clock. Chip "U" pin 7 outputs the bit clock which is 10X the byte frequency. The output of decade counter "X" and selector "U" pin 9 are fed into phase-detector "C". Chip "C" MC4044 consists of a phase-detector, a charge pump, and an amplifier. When all the negative transitions on R, the reference input, and V, the feedback input coincide, phase lockup occurs. When the lockup occurs, both outputs U1 and D1 remain high. The circuit responds only to transitions and not to input waveform duty cycle. If R leads V, output U1 pulses while output D1 remains high. When PU is low (pulsing) and PD is high, the DC voltage, at the amplifier output pin 8, will rise. If V leads R, the reverse is true.

The phase detector amplifier output is fed into varactor diode CR7. CR7, L10 and trimmer capacitor C30 form a resonant tank which controls the output frequency of oscillator "J". As the phase detector increases its DC output voltage, the capacitance of varactor diode CR7 decreases resulting in an increase in the resonant tank and VCO output frequency. Chip "N" MC10125 converts the ECL output of oscillator "J" to TTL levels for clocking the ÷N counters.

Parallel to Serial Converter

When decade counter "X" overflows, pin 15 goes to a high logic level which produces the feedback signal to the phase detector and also the load signal to the parallel to serial converter chip "AC". When "AC" pin 19 is high, byte data from the D-Port receivers is loaded into "AC" on the positive edge of the bit clock pin 12. With the load pulse high, the same clock pulse which loads "AC" also clears "AF". The clearing of "AF" produces the start-bit for the next byte of data to be shifted out. During the next 9 bit clocks, the 8 bits of data previously loaded into "AC", and a stop-bit, shifted into "AC" because pin 11 is held high, are shifted through "AF" and into TTL to ECL level converter "AR".

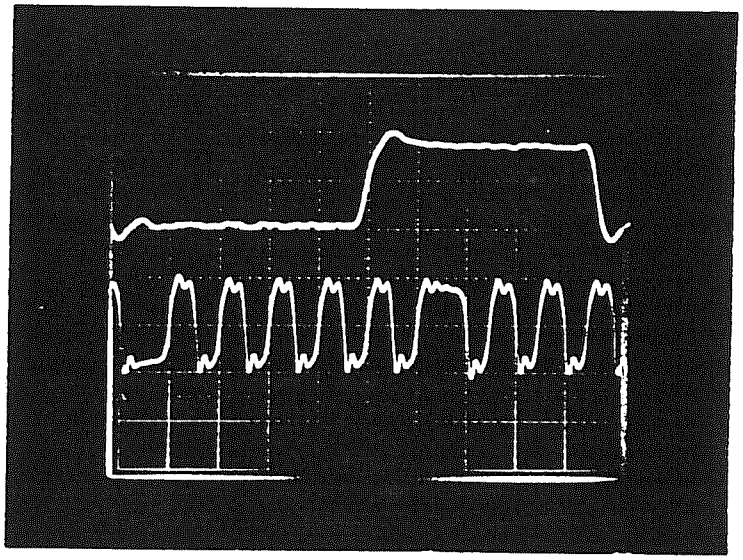
NRZ to Manchester ENcoder

NRZ data from converter "AR" goes directly to the data input of two storage registers chip "AK". The data on the inputs to "AK" is transferred to the Q outputs on the positive edge of the bit clock signal from level converter "AR".

During the low portion of the clock signal, the state of register "AK" is reversed by the outputs of gates "AL".

Transmitter

The output of storage register "AK" through gate "AV" drives the differential inputs of the fiber-optic transmitter. The transmitter is capable of outputing approximately 8 uW into a 50 um cable and 35 uW into a 100 um cable.



BYTE CLOCK TP3

WAIT BYTE TP5

20NS/CM
PHOTO 4: WAIT BYTE AT TP5

A zero-bit at TP5, the transmitter output test point, has a positive transition at the center of the bit cell time. A one-bit has a negative transition at the center of its cell time; therefore, the second half of a zero-bit cell time is always positive and the second half of a one-bit cell time is always negative (see Photo 4).

RECEIVER SECTION

The receiver section of the Model 3939 Fiber Optic U-Port converts light impulses received at the FO IN connector to a biphase voltage signal, separates this signal into 10-bit NRZ data and clock signals, frames it into 8-bit data bytes, and along with a byte clock outputs it to the D-PORT OUT connector J1.

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The receiver section consists of four main parts:

1. Fiber-Optic Receiver
2. The data separator
3. The sync circuitry
4. The serial to parallel converter

FIBER OPTIC RECEIVER

Light from the optical fiber is converted to a differential ECL voltage by the receiver module. The receiver has an input sensitivity range of 1.3 uW (-29 dBm) to 150 uW (-8 dBm).

DATA SEPARATOR

The biphase data from the receiver module goes to dual-edge detector chip "Z" which produces approximately 5 nanosecond pulses into "AND" gate "AE". The output of "AND" gate "AE" triggers monostable multivibrator "AM". Capacitor C31 is used to adjust the timing of one-shot "AM" to give the correct clock/data phase relationship at the input to latch "W". The ECL output of latch "W" (separated NRZ data) and one-shot "AM" (NRZ clock) are converted to TTL levels by chip "R".

SYNC CIRCUITRY

The sync circuitry will be explained with the use of schematic D5535, the listing for PROM "H" (see page 13), and the 3939 byte sync timing diagram shown on page 12 of this manual.

Chips "K", "L", "H", and associated gates, form a state machine which controls the framing of bit-serial data into byte-serial data. This state machine also produces a byte clock and a no-sync signal. The state machine may power up at any address (0-31). When clocks are produced as a result of incoming data, the sequencer will find a sync error and go to address 0. Chip "K" is then cleared (pin 9 low) and further clocking in inhibited. The sequencer now waits for a "START" bit. A "START" bit follows the only negative transition in an NRZ wait-byte. Upon receiving this transition, "K" pin 9 is set high and "K" pin 6, along with gate "P", produce half frequency sequencer clocks (B1-B5). Keeping in mind a wait-byte consists of six zeros followed by four ones, the sequencer must now find this pattern before byte sync can be established. As address register "L" is clocked, incoming NRZ data is used as address bit 0 of PROM "H. One can see from the PROM listing and byte sync timing that if incoming data is in the wrong state for a given clock pulse, the sequencer goes to address 0 and the process begins anew.

Once byte sync has been established, it is maintained by checking only the "STOP" bit.

If sync is maintained, a byte clock is produced at chip "L" output 10, and the no-sync signal to timer chip "D" goes away.

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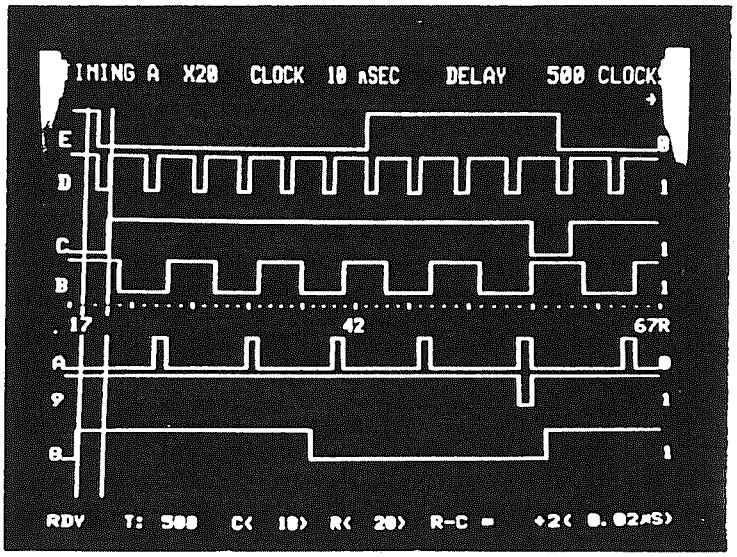
SERIAL TO PARALLEL CONVERTER

Shift register "S" stores the incoming serial NRZ data stream. The sequencer PROM "H" pin 9, and signal B5, clocks register "AG" when the 8 bits of byte data are positioned properly within shift register "S". Data from register "AG" and the byte clock are presented at the D-OUT connector J1 by differential drivers "AS", "AT", and "AU".

3939 BYTE SYNC TIMING DIAGRAM



E	NRZ wait-byte at "L" pin 6
D	Clock at "G" pin 13
C	"K" pin 9
B	"K" pin 6
A	B1 through B5 at "L" pin 9
9	Clear to chip "K"
8	Byte clock out at "AS" pin 1.

```
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DX1:PROM39.DAT to TT:


    3939 BYTE SYNC PROM
   I.C. LOCATION "H"                                10-JAN-85
-------------------------------------------------------------
   AAAAA        QQQQQQQQ
   43210  HEX   76543210    COMMENT          B-SIG.
-------------------------------------------------------------
 0-00000    01--00000001---START WAIT------B1
 1-00001    01--00000001---BYTE SEQ  ------B1
 2-00010    02--00000010---1ST "0"   ------B2
 3-00011    C0--11000000---RETURN    ------B2
 4-00100    03--00000011---2ND "0"   ------B3
 5-00101    C0--11000000---RETURN    ------B3
 6-00110    04--00000100---3RD "0"   ------B4
 7-00111    C0--11000000---RETURN    ------B4
 8-01000    C0--11000000---RETURN    ------B5
 9-01001    85--10000101---1ST "1"   ------B5
10-01010    C0--11000000---RETURN    ------B1
11-01011    06--00000110---2ND "1"   ------B1
12-01100    37--00110111---NORMAL    ------B2
13-01101    37--00110111---SYNC      ------B2
14-01110    38--00111000---OPERATING ------B3
15-01111    38--00111000---RANGE     ------B3
16-10000    39--00111001--- "         ------B4
17-10001    39--00111001--- "         ------B4
18-10010    AA--10101010--- "         ------B5
19-10011    AA--10101010--- "         ------B5
20-10100    E0--11100000---RET.STOP=0------B1
21-10101    26--00100110---NEXT BYTE ------B1
22-10110    C0--11000000---NOT USED GO TO START
23-10111    C0--11000000---   "
24-11000    C0--11000000---   "
25-11001    C0--11000000---   "
26-11010    C0--11000000---   "
27-11011    C0--11000000---   "
28-11100    C0--11000000---   "
29-11101    C0--11000000---   "
30-11110    C0--11000000---   "
31-11111    C0--11000000---   "
        !       !!!!!!!!
NRZ DATA        !!!!!!!A1
                !!!!!!A2
                !!!!!A3
                !!!!A4
                !!!BYTE CLOCK
                !!NO-SYNC
                !CLEAR "M"
               CLEAR "C"
     ACTIVE:---HHLLHHHH
```

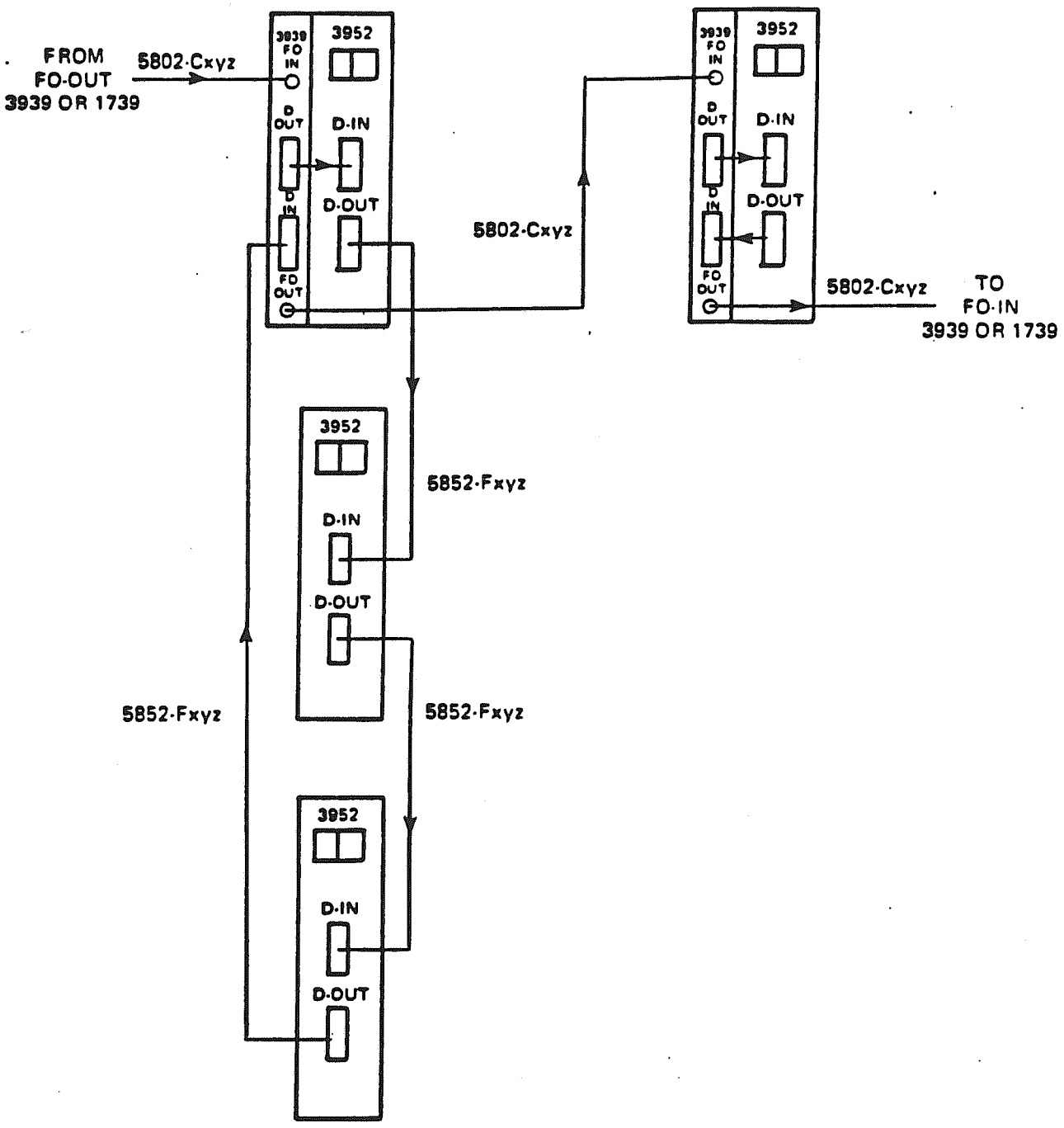

FIGURE 1: 3939 AND CRATE CLUSTER

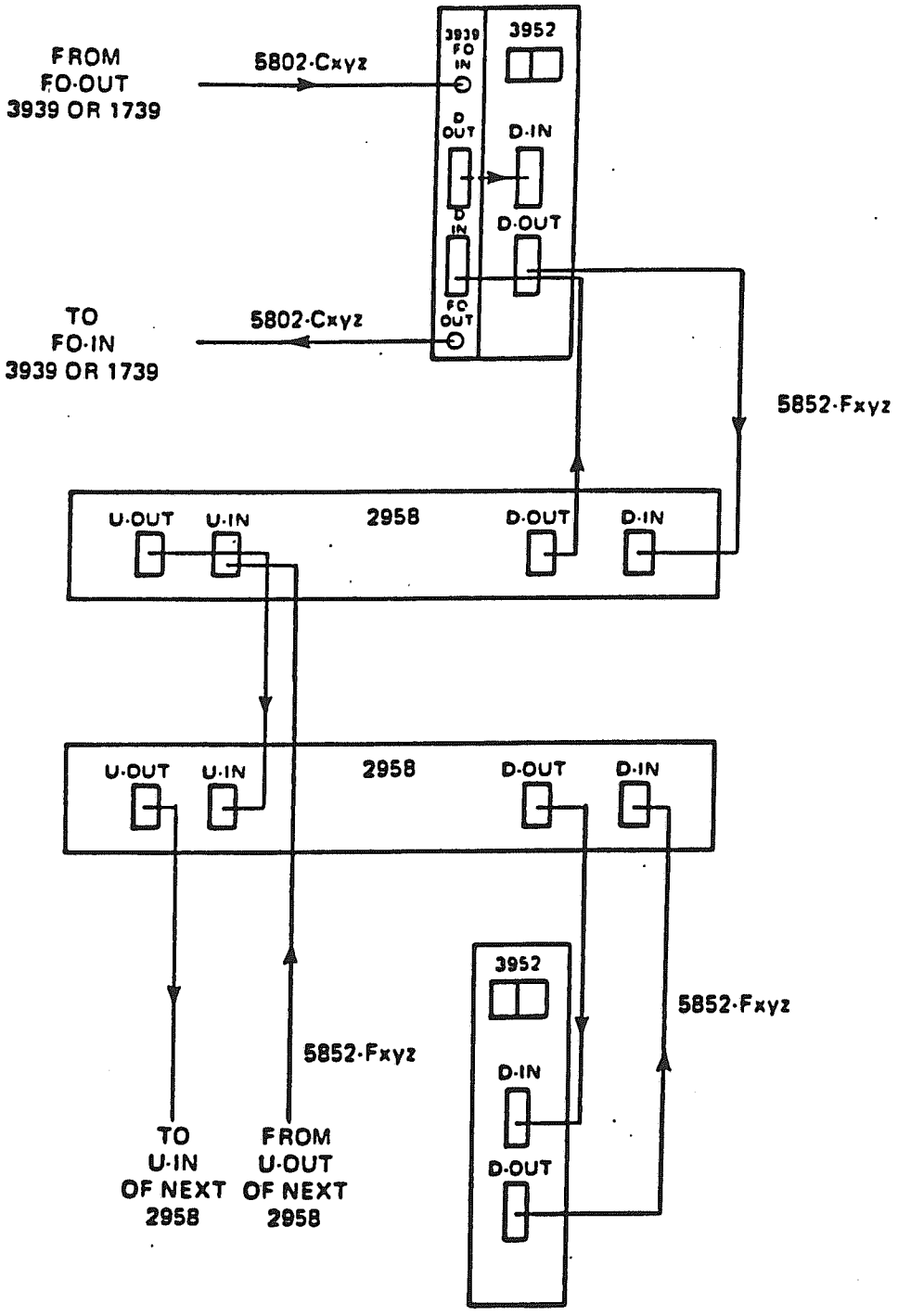

Figure 2: 3939 - 2958 SYSTEM

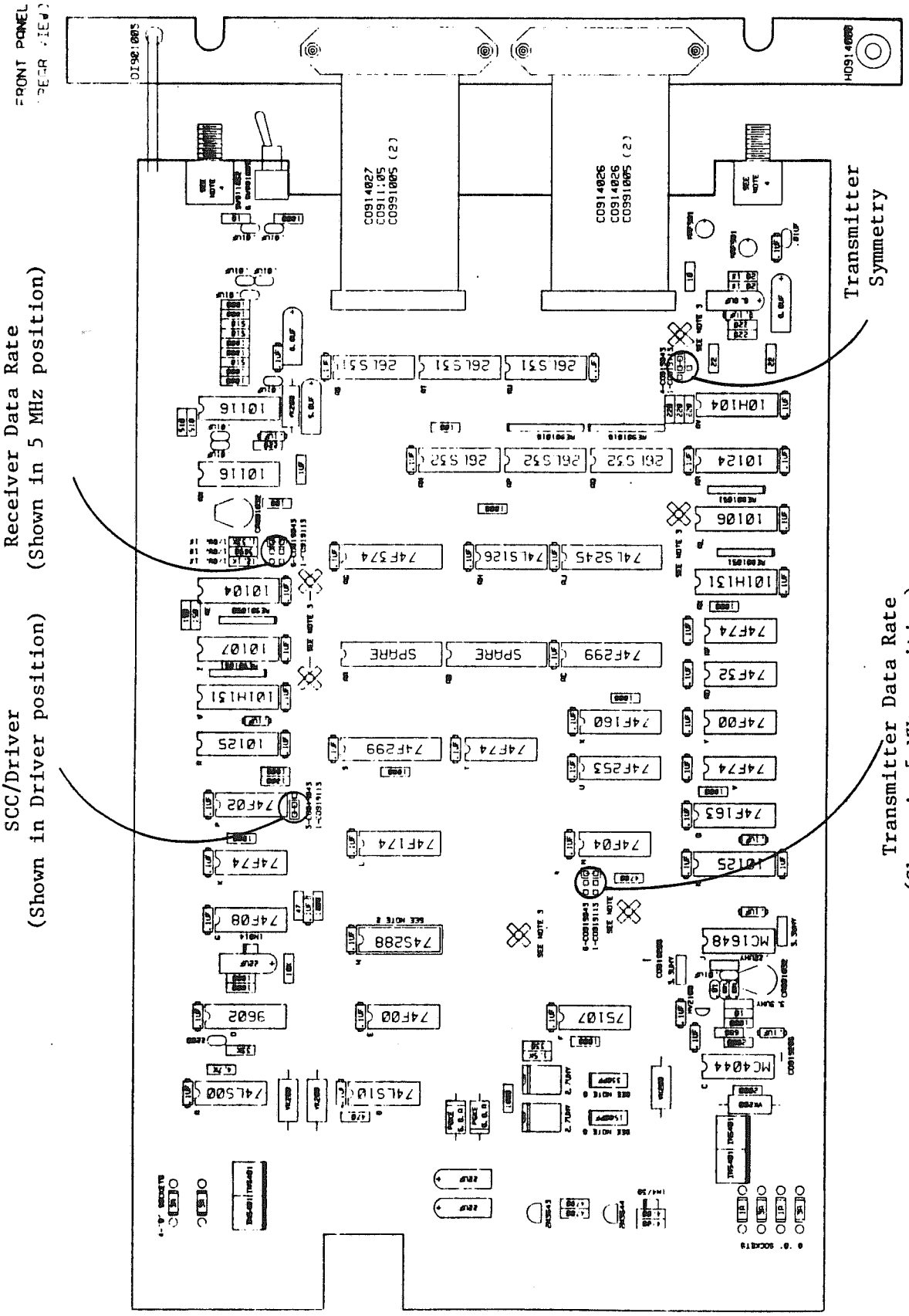

FIGURE 3: STRAP OPTIONS

WARRANTY

KineticSystems Company, LLC warrants its standard hardware products to be free of defects in workmanship and materials for a period of one year from the date of shipment to the original end user. Software products manufactured by KineticSystems are warranted to conform to the Software Product Description (SPD) applicable at the time of purchase for a period of ninety days from the date of shipment to the original end user. Products purchased for resale by KineticSystems carry the original equipment manufacturer's warranty.

KineticSystems will, at its option, either repair or replace products that prove to be defective in materials or workmanship during the warranty period.

Transportation charges for shipping products to KineticSystems shall be prepaid by the purchaser, while charges for returning the repaired warranty product to the purchaser, if located in the United States, shall be paid by KineticSystems. Return shipment will be made by UPS, where available, unless the purchaser requests a premium method of shipment at their expense. The selected carrier shall not be construed to be the agent of KineticSystems, nor will KineticSystems assume any liability in connection with the services provided by the carrier.

The product warranty may vary outside the United States and does not include shipping, customs clearance, or any other charges. Consult your local authorized representative or reseller for more information regarding specific warranty coverage and shipping details.

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1. Contact KineticSystems and discuss the problem with a Technical Service Engineer.
2. Obtain a Return Authorization (RA) Number.
3. Initiate a purchase order for the estimated repair charge if the product is out of warranty.
4. Include a description of the problem and your technical contact person with the product.
5. Ship the product prepaid with the RA Number marked on the outside of the package to:

KineticSystems Company, LLC
Repair Service Center
900 North State Street
Lockport, IL 60441

Telephone: (815) 838-0005
Facsimile: (815) 838-4424
Email: tech-serv@kscorp.com