Model 3664-L1A

Time Interval Counter

INSTRUCTION MANUAL

April, 1992

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# \*\*\*\*SPECIAL OPTION\*\*\*

Model~3664-S002

Time Interval Counter

REVISED June, 1991

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#### \*\*\*SPECIAL OPTION\*\*\*

### **REVISED JUNE, 1991**

The Model 3664-S002 is the same as Model 3664-L1A with the following exceptions:

- 1. After issuing the F(25)A(0) Initiate Command, the first positive edge detected on each channel will start the time interval counter. The Interval Accumulator will be incremented until the first positive edge following the overflow of the input pulse counter. Therefore, input cycles are counted instead of input pulses.
- 2. The input circuits of channels 1 through 5 have been changed to accept a AC coupled signal with peak-to-peak values of 1.5 to 5 volts.
- 3. Straps "A" and "B" are used to select a pulse whose leading edge is positive going.

JRH:rem(WP) June 27, 1991

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# **Time Interval Counter**

# Measures the intervals from a common start pulse to 6 stop pulses

3664

### **Features**

- · Six independent channels
- Eight timing clock frequencies from one hertz to ten megahertz
- Capacity of 65,535 counts per channel (16-bit counters)
- 24-bit time resolution per channel (maximum of 1 part in 16,777,215)
- · Individual LAM status for interrupts

## **Typical Applications**

- · Time-to-digital conversions
- Frequency determination of input pulse trains

### General Description (Product specifications and descriptions subject to change without notice.)

The 3664 is a single-width CAMAC module containing six channels of time interval counters. Data from the module can be used to represent the time elapsed between a Start and a Stop pulse, or it can be used to determine the average frequency of an input pulse train. Each channel contains a 24-bit time interval accumulator and a 16-bit, presettable input pulse counter. Latches are provided to hold the count, thereby eliminating the need to continuously rewrite the pulse counters. Time intervals are derived from a common, crystal-controlled clock on the module having Dataway selectable frequencies ranging from one hertz to ten megahertz in decade steps. Once the timing cycle has been initiated (via front-panel input signal or Dataway command), the accumulators record timing information until the preset number of input pulses has been received by the 3664. The overflow from each channel's input pulse counter or time interval counter stops the timing sequence and sets a LAM Status bit for that channel. A LAM Mask register allows any LAM stats bit or combination of bits to generate a LAM Request on the Dataway.

The common Start signal and the six pulse inputs are made via single-pin LEMO connectors on the module front panel. The Start signal is a low-true, TTL level pulse which initiates the timing cycle on the high-to-low transition. Strap selections allow use of either TTL level or optically isolated input pulses, with pulse counting activated on the low-to-high transition. The maximum frequency of the pulse inputs is five megahertz, and each input sinks 15 milliamperes of current.



### **Function Codes**

Command		Q	Action				
F(0)·A(i)	RD1	1	Reads the contents of the time interval accumulator and clears the LAM status bit for the selected channel. (See Note 1.)				
F(1)·A(12)	RD2	1	Reads the LAM status bits.				
F(2)·A(i)	RC1	1	Reads and clears the contents of the time interval accumulator and clears the LAM status bit for the selected channel. (See Note 1.)				
F(8)·A(15)	TLM	LR	Tests for the presence of a LAM request.				
F(16)·A(i)	WT1	1	Writes the number of input pulses over which time increments are to be accumulated and clears the time interval accumulator and LAM status bit for the selected channel. (See Note 1.)				
F(17)·A(0)	WT2	1	Selects one of eight timing clock frequencies (100-107 hertz) and clears all time interval accumulators and LAM status bits. (See Note 3.)				
F(17)·A(13)	WT2	1	Writes the LAM Mask register.				
F(25)·A(0)	XEQ	1	Initiates the timing cycle for all channels on the module. (See Note 4.)				
Z	CZ	0	Clears the accumulator, pulse counter, and LAM status bit on each channel and sets the timing clock frequency to one hertz.				

Notes: 1. i can range from 0 to 5.

2. X = 1 for all valid addressed commands.

A = 1 for all valid addressed commands.
Default frequency on initialization is one hertz.
All channels must be finished counting before another start command can be asserted.

### **Front Panel Indicators**

N: Flashes whenever the module is addressed

L: Indicates that a LAM Request is pending

## **Power Requirements**

+6 volts:

2.8 A

# **Ordering Information**

Model 3664-L1A

Time Interval Counter, 6 channels, with LEMO connectors

### **Related Products**

Model 5910-Z1A

Single-pin LEMO Connector

Model 3664-L1A (Rev. 12/87)

#### **OPERATION**

The first step in setting up the Model 3664-LlA is setting the strap options. See the section of this manual on Strap Options for information on strap placement.

After the straps have been set, the module can be installed in the CAMAC crate. Use the F(17)A(0) command to change the timing clock frequency (Internal Accumulator timing frequency). See the section on the Clock Control Register for available frequencies.

Each channel can then be written with the desired number of overflow pulses using the F(16)A(i) commands. After the start command (initiated by either an F(25)A(0) command or by an externally applied pulse to the start input Lemo), the module will start counting all six channels.

When each channel's pulse counter overflows after counting the desired number of pulses, a LAM status bit is set for that channel and pulse counting is disabled. If the Interval Accumulator overflows before the pulse counter overflows, an ERROR condition exists indicating that the Internal Clock speed is set too fast. A LAM status bit will be set and pulse counting will be disabled.

The timed-out data can be read back in one of two ways. The F(0)A(i) command reads the content of the time interval accumulator and clears the LAM status bits for that channel. The F(2)A(i) command is the same as the F(0)A(i) command except that it will also clear the contents of the time interval accumulator for that channel.

Once all channels have finished counting, another timing cycle can be initiated with the start pulse without having to rewrite the overflow count. If the pulse overflow count is to be changed to a new overflow count, the F(16)A(i) command must be used prior to the start command.

If using the Model 3664-LlA to determine the average frequency of an input pulse train, and the applied input pulse train is a free running clock that is asynchronous with respect to the module's start pulse, one can expect to see a slightly different count returned for several samples of the pulse train. When using the Model 3664-LlA to determine the elapsed time between a start and a stop pulse, note that on the falling edge of the start pulse there is a one microsecond delay time to allow the Interval Accumulator timing frequency to synchronize with the start pulse. Also note that the pulse counting will be disabled when the Input receives a complete pulse. For example, if the Input pulse is a high true pulse, then the pulse counter will increment on the low to high transition, with overflow and pulse counting disable occurring on the high to low transition of that pulse.

Model 3664-L1A (Rev. 12/87)

#### INPUT SIGNALS

The pulse input signals are strap-selectable as either TTL or optically isolated 10V signals with a maximum current draw of 15 milliamperes. The maximum input frequency is 5 megahertz.

The start input is a low true TTL level pulse greater than 200 nanoseconds and less than 1 microsecond in width.

#### STRAP SELECTION

For low true TTL level signals, strap locations should be B, D and E. For high true TTL level signals, strap locations should be A, D and E. For low true opto-isolated signals, strap locations should be A, C, and F. For high true opto-isolated signals, strap locations should be B, C and F.

The module is sent from the factory strapped for high true TTL level signals, with locations marked A, D, and E.

### CLOCK CONTROL REGISTER F(17)A(0)

3	02	01
CLK	CLK	CLK
_3	2	11

	BIT		
03	02	01	FREQUENCY
0	0	0	1 Hz
0	0	1	10 Hz
0	1	0	100 Hz
0	1	1	l KHz
1	0	0	10 KHz
1	0	1	100  KHz
1	1	0	1 MHz
1	1	1	10 MHz

### LAM STATUS REGISTER F(1)A(12)

1	2	11	10	09	08	07	06	05	04	03	02	01
! CH	16	CH5	CH4	СН3	CH2	CH1	СН6	CH5	CH4	СНЗ	CH2	CH1 ;
int	er	inter	inter	inter	inter	inter	pulse	pulse	pulse	pulse	pulse	pulse

The LAM Status Register contains twelve LAMS: six input pulse counter LAMS and six Interval Accumulator LAMS. The pulse counter LAMS are set when the appropriate channel pulse counter overflows. The Interval Accumulator LAM indicates that the accumulator overflowed before pulse counting was completed.

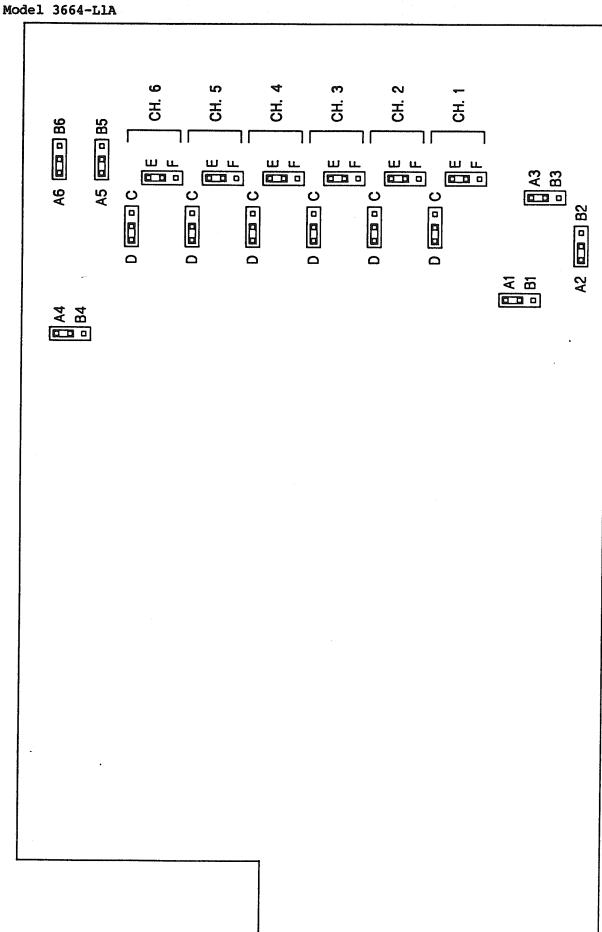
Model 3664-L1A (Rev. 12/87)

# LAM MASK REGISTER F(1)A(13)

12	11	10	09	08	07	06	05	04	03	02	01
! СН6	CH5	CH4	СН3	CH2	CH1	CH6	CH5	СН4	СНЗ	CH2	CH1
inter	inter	inter	inter	inter	inter	pulse	pulse	pulse	pulse	pulse	pulse !

The LAM Mask Register contains twelve maskable LAMS: six input pulse counter LAMS and six Interval Accumulator LAMS. The module can be masked to allow any LAM status bit or combination of bits to generate a LAM Request Signal.

WEH:rem(3000 Ser. 11)



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- 4. Include a description of the problem and your technical contact person with the product.
- 5. Ship the product prepaid with the RA Number marked on the outside of the package to:

KineticSystems Company, LLC Repair Service Center 900 North State Street Lockport, IL 60441

Telephone: (815) 838-0005 Facsimile: (815) 838-4424 Email: tech-serv@kscorp.com