Model 3395-E1A

3-channel, Digital-to-synchro Converter

INSTRUCTION MANUAL

March, 1992

****** SPECIAL OPTION ******

Model 3395-S001

Multichannel Digital-to-Synchro Converter

September, 1986

****** SPECIAL OPTION ******

Model 3395-S001

Multichannel Digital to Synchro Converter

The Model 3395-S001 is the same as the 3395-E1A except that it has been modified to provide a maximum output power of 3 volt amperes per channel instead of 1 volt ampere per channel.

September, 1986

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FIGURES

Schematic Drawing # 022180-D-4596

See Reply Card Following Warranty

Warranty

JRH:JPS:rem

KineticSystems Corporation

Standardized Data Acquisition and Control Systems **3395**

Multichannel Digital-to-Synchro Converter

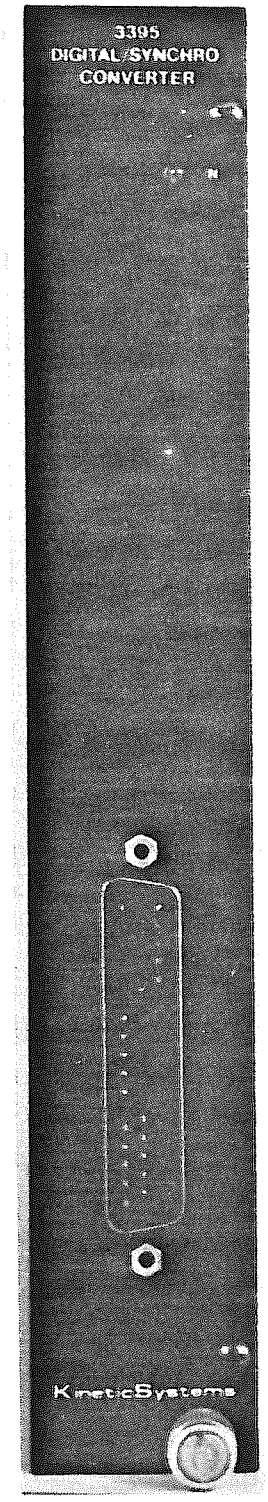
Feb. 86

FEATURES

- **Multichannel Digital-to-Synchro Converter module with 16-bit resolution**
- **Total cumulative output error is less than ±4 arc-minutes**
- **Write data packing for maximum throughput**
- **Rank1/Rank 2 registers for simultaneous conversion**

APPLICATIONS

- **Driving control transformers**
- **Positioning control systems**



GENERAL DESCRIPTION

The Model 3395 Digital-to-Synchro Converter module provides an interface between the CAMAC Dataway and standard 3-wire synchro receivers, allowing the computer to control a device's angular position. It is a double-width module with three DSC channels; each channel contains a separate converter with 16 bits of resolution. The DSC outputs are brought to a 50-pin "D"-type connector on the front panel.

The module accepts straight binary data that represents the desired angles (0 to 360 degrees) from the CAMAC Dataway in a packed format. This data is loaded, by CAMAC commands, into the Rank 1 register for each channel. The Rank 1 data is simultaneously loaded into the Rank 2 registers so that all DSCs are updated at once.

OPERATION

The data is written into the Rank 1 registers via F(16) commands. For maximum throughput, the data is packed in the full 24 bit word, as follows:

F(16)·A(0)	W24 = CH1 MSB	W9 = CH1 LSB	W8 = CH2 MSB
F(16)·A(1)	W17 = CH2 LSB	W16 = CH3 MSB	W1 = CH3 LSB

The external control of the Rank 2 register (and DSC) update is selected by the Mode register. Then Rank 1 data is copied to the Rank 2 register by a one microsecond pulse on the P1 or P2 Dataway lines. There are 7 modes of external Rank 1/Rank 2 update control, determined by the contents of the External Mode Control register. This register shall be written by an F(17)·A(0) command using Dataway bits W1-W3 (W1-LSB). Rank 1 data may be copied to Rank 2 register by F(25)·A(0), command regardless of the mode setting.

MODE CONTROL REGISTER

Mode	External Control of Rank 1/Rank 2 Transfer
0 to 3	Disabled
4	P1 or P2 clock pulse
5	P2 clock pulse
6	P1 clock pulse
7	P2 pulse, followed by P1 pulse

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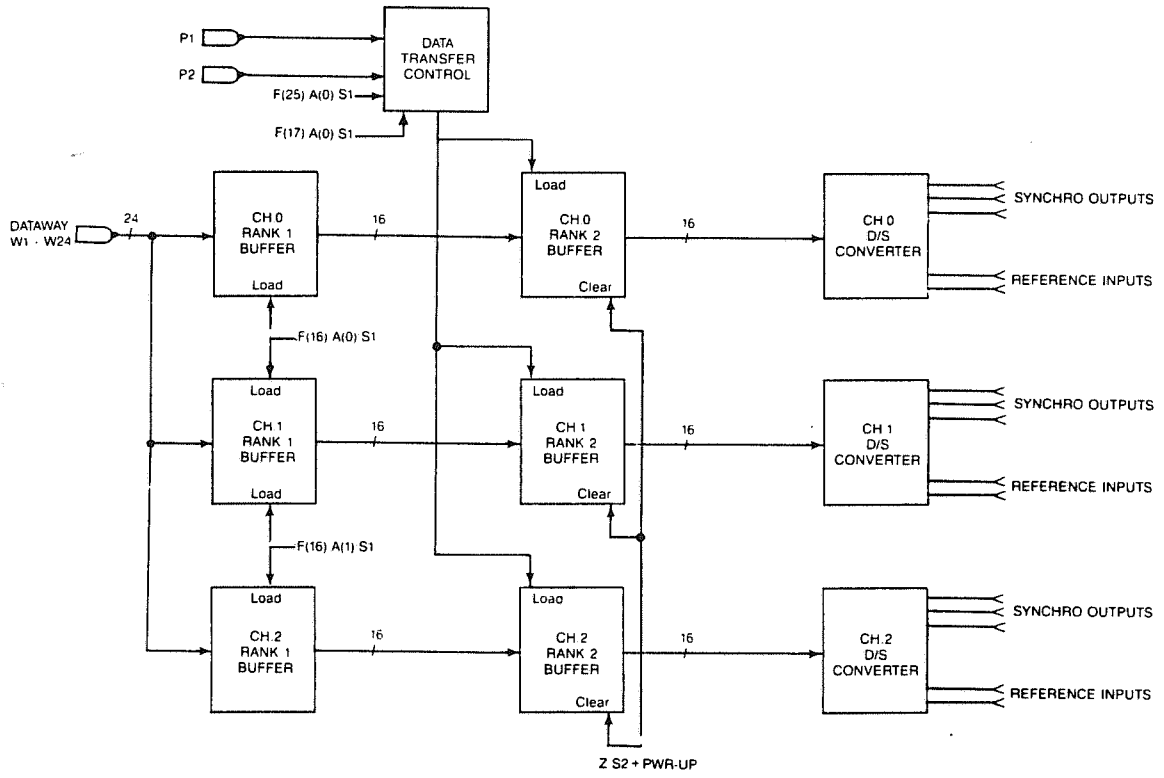
FUNCTION CODES

Command		Q	Action
F(16)·A(0)	WT1	1	Writes channel 1 and high order channel 2 data to Rank 1 registers.
F(16)·A(1)	WT1	1	Writes low order channel 2 and entire channel 3 data to Rank 1 registers.
F(17)·A(0)	WT2	1	Writes External Mode Control register.
F(25)·A(0)	XEQ	1	Executes a Rank 1/Rank 2 data transfer on all channels.
Note: X = 1 for all valid addressed commands.			

SIMPLIFIED BLOCK DIAGRAM



SPECIFICATIONS (For each channel, 25 degrees C, except where noted.)

Resolution:	16 bits
Reference signal input:	26 Vrms, 400 Hz
Output rating:	11.8 Vrms line-to-line at 400 Hz
Settling:	To within ½ LSB within 50 microseconds with a 179 degree step
Performance:	Monotonic to 14 bits, 15 ro 35 degrees C
Total cumulative error:	Less than ±4 arc-minutes
Output drive:	1.3 volt ampere MAX

POWER REQUIREMENTS

+6 volts — 250 mA
+24 volts — 350 mA
−24 volts — 550 mA

ORDERING INFORMATION

Weight: 1.03 kg. (2 lb. 5 oz.)

Model 3395-E1A — 3-Channel 16-Bit Digital-to-Synchro Converter
Accessories — Model 5934 Mating Connector

SYSTEM SETUP

The DSCs used on the 3395-E1A are designed for a 400 Hz reference frequency with a 26 volt RMS reference voltage ±10%. Outputs are rated for an output of 11.8 volts RMS line-to-line signal voltage with a maximum drive capability of 1.3 volt-ampere.

Output connections to the 3395-E1A should be kept as short as possible. At distances less than 25 feet, twisted wire is preferred. For distances greater than 25 feet, it is advisable to use individually shielded multicore wire.

DATA FORMAT

The 3395-E1A accepts straight binary representation of the desired angles (0 to 360°) from the CAMAC Dataway using F16 commands. Figure 1 shows the bit weight for word lengths of 16 bits.

Bit No.	Angle in Degrees/Decimals	Angle in		
		Degrees	Arc. Mins.	Arc. Secs.
B15 MSB	180.00000	180	0	0.0
B14	90.00000	90	0	0.0
B13	45.00000	45	0	0.0
B12	22.40000	22	30	0.0
B11	11.25000	11	15	0.0
B10	5.62500	5	37	30.0
B9	2.81250	2	48	45.0
B8	1.40625	1	24	22.5
B7	0.70313	0	42	11.3
B6	0.35156	0	21	5.6
B5	0.17578	0	10	32.8
B4	0.08790	0	5	16.4
B3	0.04395	0	2	38.2
B2	0.02197	0	1	19.1
B1	0.01099	0	0	39.6
B0 LSB	0.00549	0	0	19.8

FIGURE 1

The input data is in packed format with each channel's data left justified in a 16-bit field. Subaddress A(0) and A(1) are assigned and data shall be written in the format shown in Figure 2.

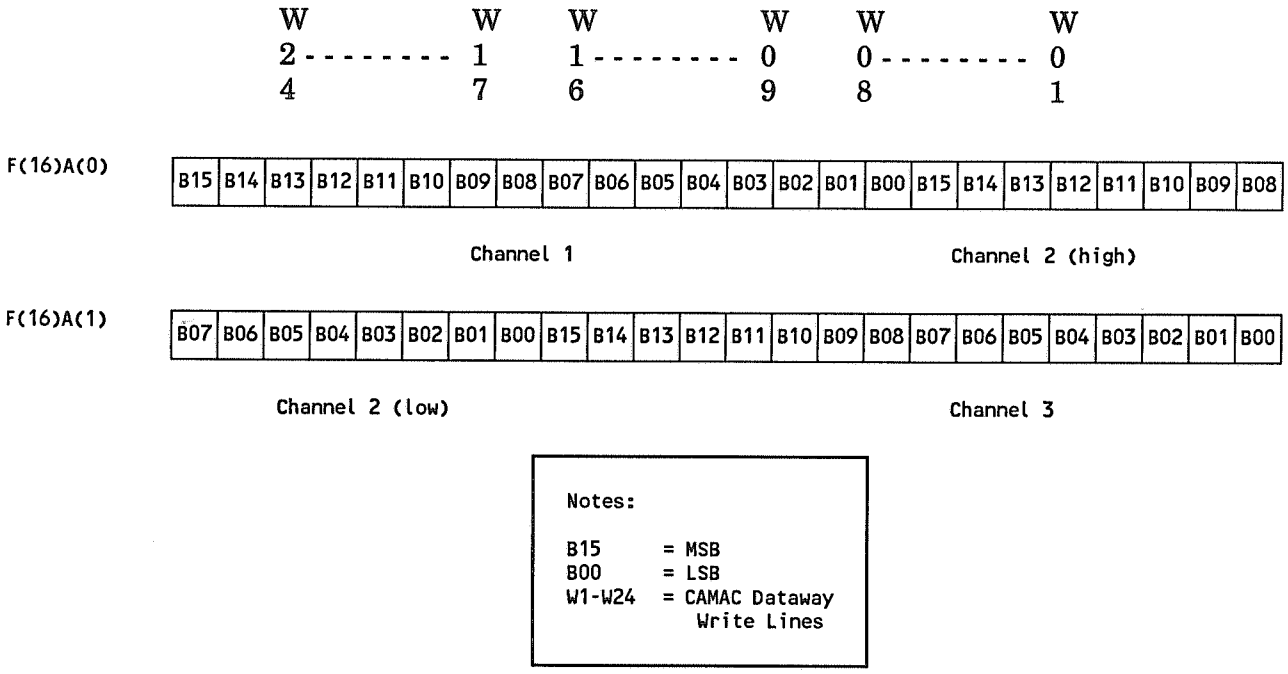


FIGURE 2

UPDATE CONTROL

After the F(16) write commands, the data will stay in the Rank 1 registers (see simplified block diagram) until a Rank 2 register update pulse is received. The Rank 1 data is then simultaneously loaded into the Rank 2 register so that all DSCs are updated at the same time.

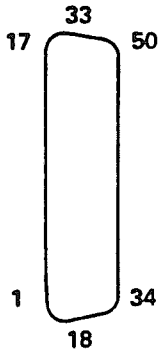
The updating of the Rank 2 registers is controlled by the Mode Control Register. This register responds to a F(17)A(0) command using Dataway bits W1-W3 (W1-LSB). Rank 1 data is copies to the Rank 2 register by an externally applied one-microsecond pulse to the P1 or P2 free Dataway bus line. Figure 2 shows each mode of operation and the function that causes a Rank 2 update. Rank 1 data may also be copied to the Rank 2 register by an F(25)A(0) command regardless of the mode settings.

Mode	Bits (W3-W1)	External Control of Rank 1/Rank 2 Transfer
0 to 3	(000-011)	Unused modes
4	(100)	P1 or P2 clock pulse
5	(101)	P2 clock pulse
6	(110)	P1 clock pulse
7	(111)	P2 pulse, followed by P1 pulse

NOTE: Upon initialization, the Mode Register is set to mode 7.

FIGURE 3

3395-E1A Pin Wire List



FACE VIEW

50 PIN 'D'

PIN NO.		PIN NO.		PIN NO.	
17	DIGITAL GROUND	33		50	DIGITAL GROUND
16		32		49	
15		31		48	
14		30		47	
13		29		46	
12		28		45	
11	CHANNEL 2 S3	27		44	
10	CHANNEL 2 S2	26		43	
9	CHANNEL 2 S1	25		42	
8	CHANNEL 2 RL	24		41	
7	CHANNEL 2 RH	23		40	
6		22	CHANNEL 3 S3	39	
5	CHANNEL 1 S3	21	CHANNEL 3 S2	38	
4	CHANNEL 1 S2	20	CHANNEL 3 S1	37	
3	CHANNEL 1 S1	19	CHANNEL 3 RL	36	
2	CHANNEL 1 RL	18	CHANNEL 3 RH	35	
1	CHANNEL 1 RH			34	